EXPERIMENT 3: TTL AND CMOS CHARACTERISTICS

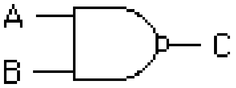
PURPOSE

Logic gates are classified not only by their logical functions, but also by their logical families. In any implementation of a digital system, an understanding of a logic element's physical capabilities and limitations, determined by its logic family, are critical to proper operation. The purpose of this experiment is to provide an understanding of some of the characteristics of the transistor-transistor logic (TTL) family and Complementary Metal Oxide Semiconductor logic (CMOS) family.

TTL FAMILY

The *logic family* refers to the general physical realization of a logical element, such as the TTL, emitter-coupled logic (ECL), or complementary metal-oxide semiconductor (CMOS) logic families. Within each logic family are one or more *logic series* that have distinctive characteristics, relative to other series within the same logic family. For example, in the TTL logic family, there are several logic series: the 74 standard, 74L low-power, 74H high-speed, 74S standard Schottky, 74LS low-power Schottky series, and 74ALS advanced low-power Schottky series.

The TTL family was the most widely used logic family for several years, characterized by its relatively high speed operation. However, it has now been largely replaced by CMOS logic. The physical representation of the binary logic states in these families are high and low voltages, as described in Experiment 1. Assuming positive logic, in the 74LS TTL family LOW (L) voltages in the range 0 V to 0.8 V are considered to be logic 0, and HIGH (H) voltages in the range 2.0 V to 5.5 V are considered to be logic 1. Figure 3.1 illustrates the voltage levels for all possible input combinations to a two-input TTL NAND gate.



A	B	C
L	L	H
L	H	H
H	L	H
H	H	L

Figure 3.1 Voltage Level Table for a Two-input TTL NAND Gate.

You may wonder why the NAND gate is so popular in the TTL logic families. Perhaps the most important factor in the use of such gates is the presence of transistors. Transistors are *active* devices that tend to restore signal levels and preclude signal deterioration which could cause 1 and 0 become indistinguishable. No degradation of signal levels occurs, even for long chains of TTL NAND gates. In the TTL family the number of transistors required to implement a NAND gate is less than that required to implement other gates such as AND, OR and NOR. Another factor in favor of NAND gates is the fact that any combinational logic function can be realized using just NAND gates.

TTL CHARACTERISTICS

Each logic family is characterized by several important parameters. These properties, and how they relate to the TTL logic family in particular, are explained below:

Fan-in is the maximum number of inputs to a gate. Although physical considerations limit fan-in, more pragmatic factors, such as limitations on the number of pins possible on IC packages and their standardization predominate. TTL NAND gates typically provide 1, 2, 4, or 8 inputs. If more than eight inputs are required, then a network of NAND gates must be employed.

Fan-out specifies the number of standard loads that the output of a gate can drive without impairing its normal operation. A standard load is defined to be the amount of current required to drive an input of another gate in the same logic family. Due to the nature of TTL gates, two different fanout values are given, one for HIGH outputs and one for LOW outputs. Typically when an input is at logic 1 at most 40μA flows into an input ($I_{IH(max)}$, see Lab 1), and it must be provided (sourced) by the driving output. For logic 0, at most 1.6 mA flows from the input (I_{ILmax}), which the driving output must "sink". By convention the current flowing into an input or output is considered positive while a current flowing out of an input or output is considered negative; hence, I_{ILmax} = -1.6mA. A typical TTL gate can source 400 μA ($I_{0H(max)}$) of current and can sink 16 mA ($I_{0L(max)}$). Hence TTL gates typically have a HIGH (logic level) fanout of

$$|I_{0H(max)}/I_{IH(max)}| = |-400\ \mu A\ /\ 40\ \mu A| = 10,$$

and a LOW fanout of

$$|I_{0L(max)}/I_{IL(max)}| = |16\ mA\ /\ -1.6\ mA| = 10.$$

Exceeding these fan-out limits may result in incorrect voltage levels at the output, as a gate cannot provide or sink enough current. The lower value of the two fanout values determines the fanout of the gate. In the case of 7400 TTL logic, they are equal, but for some other types of

TTL logic the limiting value is the LOW fanout. Some TTL structures have fan-outs of at least 20 for both logic levels.

A **voltage transfer curve** is a graph of the input voltage to a gate versus its output voltage; Figure 3.2 shows the transfer curve for TTL inverter without any fanout. When the input voltage is 0 V, the output is HIGH at 3.3 V. As the input voltage is increased from 0 to 0.7 V, the output remains relatively constant (Region I). Beyond 0.7 V to about 1.2 V, the output decreases more gradually with increasing input voltage (Region II). The *threshold voltage,* the voltage on the transfer curve at which $V_{out} = V_{in}$ and occurs in Region III, is found at the intersection of the transfer curve and the line $V_{out} = V_{in}$. Finally, in Region IV, the output remains constant at 0.2 V as the input voltage is increased.

Noise immunity is a measure of the ability of a digital circuit to avert logic level changes on signal lines when noise causes voltage level changes. (See Figure 3.3.) One measure of noise immunity is characterized by a pair of parameters: the dc HIGH and LOW *noise margins*, DC1 and DC0, respectively. They are defined as follows:

$$DC1 = V_{OH(min)} - V_{IH(min)}$$

and

$$DC0 = V_{IL(max)} - V_{OL(max)}.$$

The minimum values of DC1 and DC0 determine worst case noise margin.

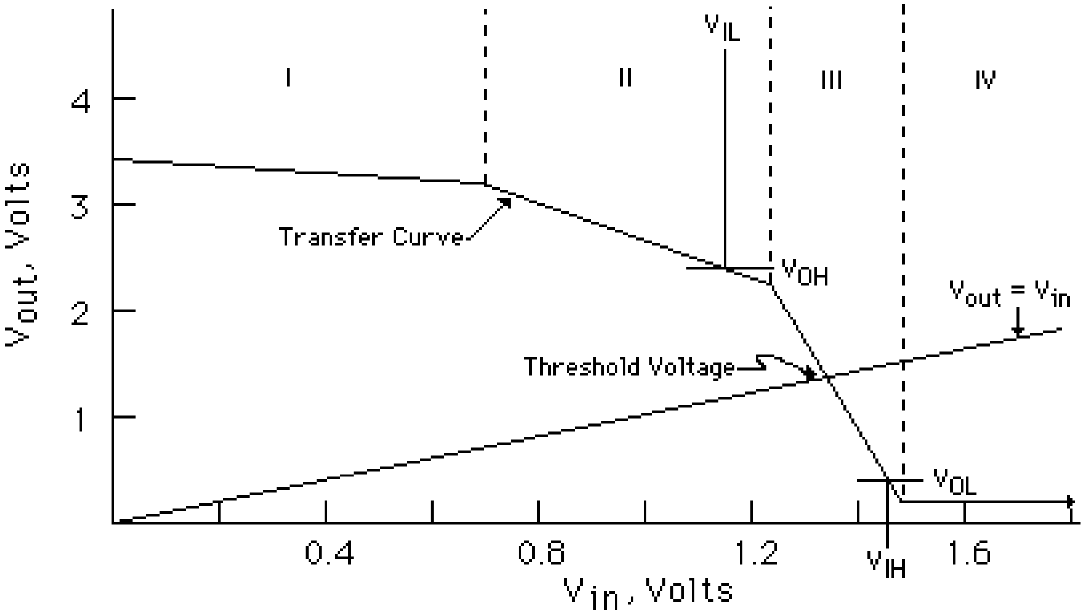


Figure 3.2 Voltage Transfer Curve for a TTL Gate.

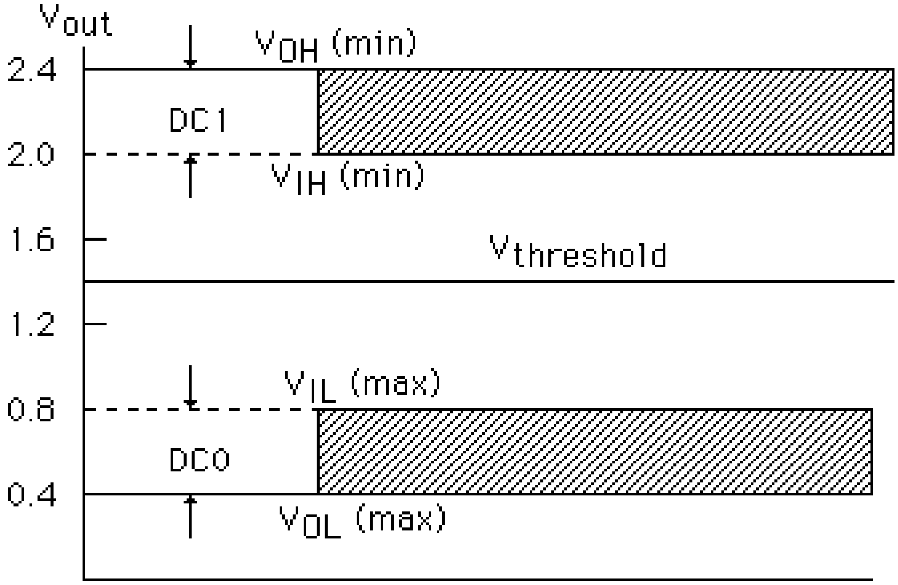


Figure 3.3 Input and Output TTL Voltage Levels Illustrating DC Noise Margin.

Recall from Experiment 1 that $V_{OL(max)}$ is the largest voltage that can occur on the output of a gate when the output is in the LOW (logic 0) voltage range. $V_{OH(min)}$ is the smallest voltage that can occur on a gate output when the output is in the HIGH (logic 1) voltage range output. In addition, $V_{IH(min)}$ is the smallest input voltage that will be interpreted as a HIGH input and $V_{IL(max)}$ is the greatest input voltage that will be interpreted as a LOW input. Note that V_{OL} and V_{OH} are specified by the manufacturer on the data sheets for the device. V_{IL} and V_{IH} can be determined, given V_{OL} and $V_{OH,}$ from the voltage transfer curve, as indicated in Figure 3.2. Illustrated in Figure 3.3 are the DC0 and DC1 noise margins. For the TTL family, typically DC0 = 0.8 - 0.4 = 0.4 V, and DC1 = 2.4 - 2.0 = 0.4 V. (The values for V_{OL}, V_{OH}, V_{IL}, and V_{IH} were obtained from the specification sheet of the 7400 NAND gate.) Any disturbance with a negative peak of up to DC1 could appear superimposed on the worst case HIGH voltage level, V_{OH}, on an input without disturbing the gate output. A similar statement can be made for DC0.

The **propagation delay time** for a gate is the time required for the output to respond to a change in an input. In all practical gates, a time lag exists between an input change and the corresponding output response. The time interval between the instants when the input and output change states is not a satisfactory measure of the delay time of a logical device for two reasons. First, the input signals to gates and the output signals produced by gates are not the idealized pulses studied in theory. Figure 3.4 illustrates the nonideal input and output signals to a NAND gate. The transitions between HIGH and LOW voltage levels have nonzero *rise* and *fall times*. The time required for a signal to rise from 10% to 90% of its final value is called the rise time, t_r.

The fall time, t_f, is the time required for the signal to fall from 90% to 10% of its initial value. Secondly, the input voltage to a gate has only to reach the threshold voltage level before the device begins to change state. For these reasons, the delay time is measured with respect to a *reference voltage level* V_{ref}, or the threshold voltage.

Consider the NAND gate in Figure 3.4, connected as a NOT gate. The input waveform, V_{in}, is a non-ideal pulse. When the input signal goes HIGH, the output will go LOW after the *turn-on delay time* t_{PHL}. The figure illustrates the turn-on delay for a non-ideal output pulse. The typical turn-on delay for a standard series TTL NAND gate is 7 ns. When the input signal goes LOW again, the output of the NAND gate goes HIGH after the *turn-off delay time* t_{PLH}. The typical turn-off delay time for a standard series TTL NAND gate is 11 ns. The average *propagation delay time* t_p is then defined by:

$$t_p = (t_{PHL} + t_{PLH}) / 2.$$

The maximum value for both t_{PHL} and t_{PLH} is 15 ns.

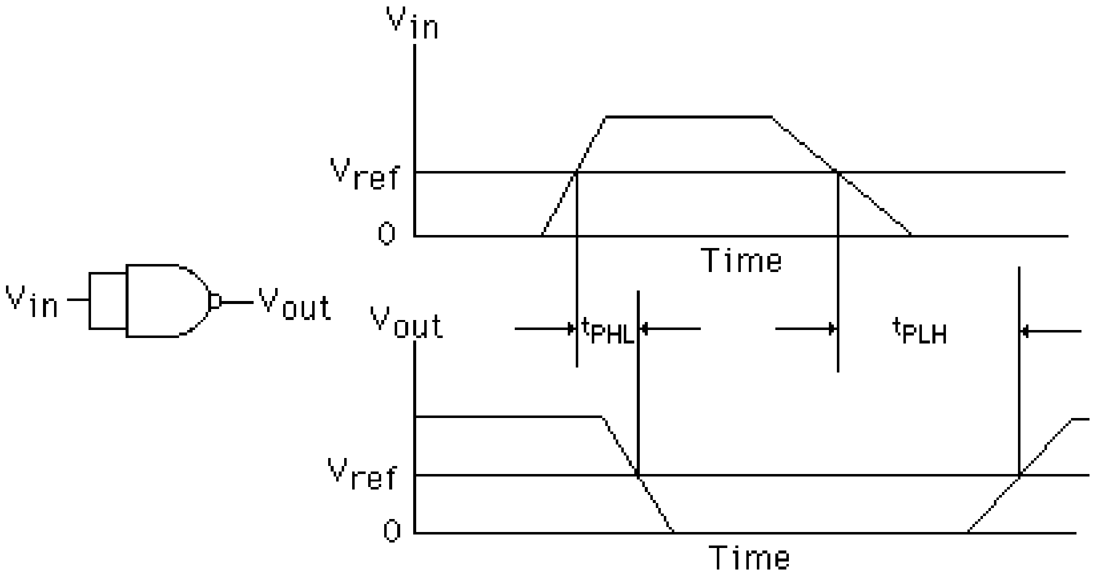


Figure 3.4 Propagation Delay Times.

A phenomenon associated with TTL devices is **current spiking**. When the output of a TTL device is HIGH, a constant supply current I_{CCH} is drawn from the power supply by the IC. When the output is LOW, a constant supply current I_{CCL} is drawn from the power supply. For a 7400 NAND gate, I_{CCH} = 4 mA and I_{CCL} = 12 mA per IC. However, when the gate output changes state, a short burst of current is drawn during the transition. The result is current spikes (narrow pulses) in the power supply line as shown in Figure 3.5. The largest spike occurs in the LOW to HIGH transition. To prevent these current spikes from corrupting the power supply and ground and thus appearing as noise, one decoupling capacitor (0.01 μF to 0.1 μF) for each five to ten IC packages are generally connected from power to ground near the IC pins.

Recall from Lab 1, it was mentioned that the power supply should never be connected directly to gate inputs as the gate could be destroyed if the input voltage ever exceeded the supply voltage to the IC--a virtually unlimited amount of current is then allowed to flow backwards through the IC. Current spiking can lead to just such a situation if power were connected directly to a gate's inputs. Thus, another TTL gate should always be used to provide a constant HIGH voltage if required.

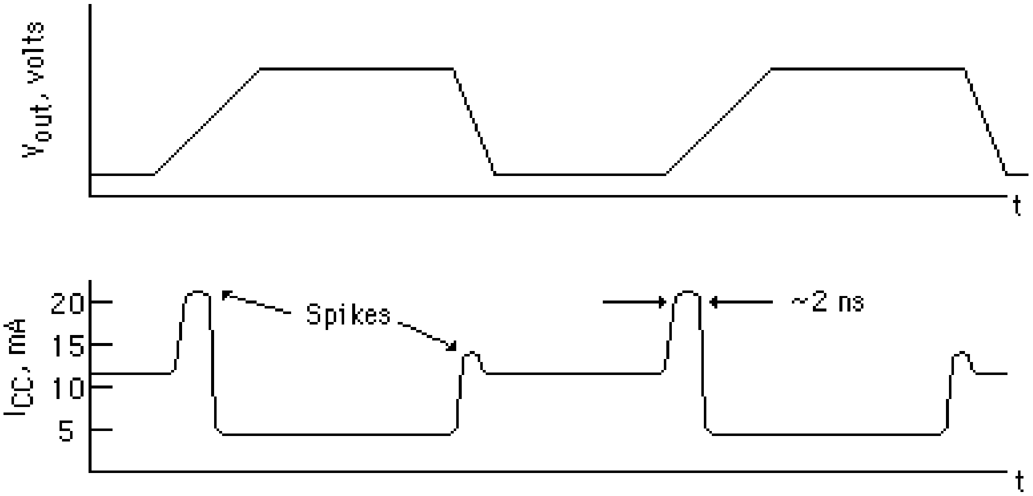


Figure 3.5 Waveforms Illustrating TTL Current Spiking.

Another important characteristic of digital IC's is their **power dissipation**. As the power dissipation in a system increases, more heat must be dissipated from the system and larger, more costly power supplies are required. The static power dissipation P_{DP} of an IC is the product of the supply voltage V_{CC} and the static power supply current I_{CC}. If, on the average, the output of a device is HIGH half the time and LOW the other half, then the average power supply current is $I_{CC} = (I_{CCH} + I_{CCL})/2$.

An unconnected input to a gate is called a **floating input**, because it floats at the threshold voltage for the device. A floating TTL input usually acts as a HIGH input. However, open inputs are susceptible to noise which can be received by an input via the package leads, which act as antennae for noise. Even a few hundred millivolts of negative noise voltage is sufficient to drive a floating input to the LOW state. Therefore, it is advisable to tie all unused inputs of any gate (when the gate has more inputs than required) to HIGH or LOW voltage. In addition, the outputs of unused gates in an IC package should be forced HIGH by appropriate connection of the inputs. This provides a convenient HIGH, reduces the power dissipation ($I_{CCH} < I_{CCL}$), and prevents oscillation of the gate's outputs, which also causes increased power dissipation and current spiking.

Any loads imposed upon the outputs of gates deteriorate the output signal. **Capacitive loading** occurs if the load impedance to the output of a gate has a capacitive component. This external load capacitance component can be caused by such things as other logic devices or stray wiring capacitance. The effect of capacitive loads is to increase the rise and fall times of signals, subsequently increasing propagation delay times and reducing the maximum operation speed. **Resistive loading** is present when the load impedance contains a resistive component, such as that associated with other logic devices. The effect of resistive loading is reduced noise margins and output voltages.

TTL gates are available in three different types of output configurations. **Totem-pole output** gates are used in most logic; in this case, the gate by itself drives its output HIGH or LOW depending on the gate's inputs. Connecting the outputs of two or more totem-pole gates together produces undefined output values, may damage the device and should never be done. **Open-collector output** gates can only drive their output LOW; for input combinations where the output should be HIGH, an external pullup resistor connected the supply voltage is needed to produce the HIGH. The outputs of open-collector gates to be wired together; the result is to effectively AND all the output signals together. Finally, **three-state** (or **tri-state**) **output** gates provide, as their name implies, three output states. Like totem-pole output gates, tri-state gates can drive their output either HIGH or LOW, as determined by the input combination, but they also have a control input that overrides the effect of the other inputs and places the gate output in a ‘third state’. In the third state the internal transistors of the gate are effectively disconnected from the gate output and the output is in an open circuit or high-impedance state. This allows a direct wire connection of many tri-state gate outputs to a common line; however, when this is done, all but at most one of the tri-state output gates connected together must be in the high-impedance state at any given time.

CMOS FAMILY

CMOS logic is exemplified by its extremely low power consumption and high noise immunity. Hence, it is prevalently used in devices demanding low power dissipation, such as digital wristwatches and other battery powered devices, or in devices operated in noisy environments, such as industrial plants. A wide variety of CMOS logic devices in the 4000 series are available.

Unlike TTL logic, CMOS logic requires two supply voltages, V_{DD} and V_{SS}. In typical logical designs, V_{DD} ranges from +3 V to +16 V. The other supply, V_{SS}, is normally grounded.

Also, the physical representation of the binary states in CMOS logic is not entirely compatible with TTL logic. As a consequence of CMOS's extremely high input impedance, the logic levels in CMOS systems are essentially V_{DD} and ground. If, for example, a 5 volt power supply is used, LOW typically ranges from 0 to 0.01 V and HIGH from 4.99 to 5.0 V for CMOS outputs. Input voltages ranging from 3.5 to 5 V are recognized as HIGH and voltages from 0 to 1.5 V as LOW.

It may appear that CMOS output logic levels, using a 5 V power supply, completely conform to the TTL logic level ranges of 0 to 0.8 V for LOW and 2.0 to 5.5 V for HIGH. However, the voltage level ranges representing HIGH and LOW are not the only factors that determine whether two logic family are compatible or not. The amount of current that can be supplied by outputs and that can be assimilated by inputs of gates within each logic family is another consideration. Specifically, when CMOS drives TTL logic, the crucial question is whether the CMOS output, in the LOW state, can sink enough of the current originating at the TTL input to ensure that the voltage at the TTL input does not exceed its maximum LOW level input voltage of 0.8 V. Typical CMOS gates can sink about 0.4 mA in the LOW state while maintaining an output voltage of 0.4 V or less. This is sufficient to drive two low-power TTL inputs, but generally insufficient to drive even one standard TTL input. In any case, loss of dc noise immunity is an inevitable result. It is better to use a special buffer such as a 74C901 to drive standard TTL from CMOS. The HIGH state poses no problems.

Similarly, improper circuit operation may result from connecting TTL outputs to CMOS inputs. In the LOW state, a TTL output can drive CMOS directly. However, the guaranteed TTL HIGH output level of 2.4 volts is not a valid input level for CMOS. If the TTL output drives only CMOS inputs, then essentially no current is drawn and the HIGH output may be 3.5 V or higher. (A pullup resistor to +5 can be connected to the gate output to assure that the output is above 3.5V.) Whether this is sufficient for reliable operation depends upon the exact specifications for both the TTL outputs and the CMOS inputs.

CMOS CHARACTERISTICS

The **voltage transfer curve** for a typical CMOS logic gate is shown in Figure 3.6. Note that the curves in the transition region are almost vertical. This narrow transition region is the reason for CMOS logic's high noise immunity. Not much voltage range is covered in the transition from one state to the other. In contrast to TTL devices, the threshold voltage depends on the supply voltage and is approximately half the supply voltage.

As with TTL logic, **current spiking** occurs during switching. Hence, bypass capacitors are used in CMOS logic design as well. However, they are not as critical as in TTL logic design because of CMOS's high noise immunity.

Whereas the typical **quiescent (static) power dissipation** (power dissipation of a device that is not changing logic states) of TTL IC's was about 40 mW, the power dissipation of CMOS IC's are typically 25 nW. However, as the frequency of switching increases, **dynamic power**

dissipation becomes important, as illustrated in Figure 3.7. Above 1 MHz, the dynamic power dissipation predominates and can exceed TTL power dissipation.

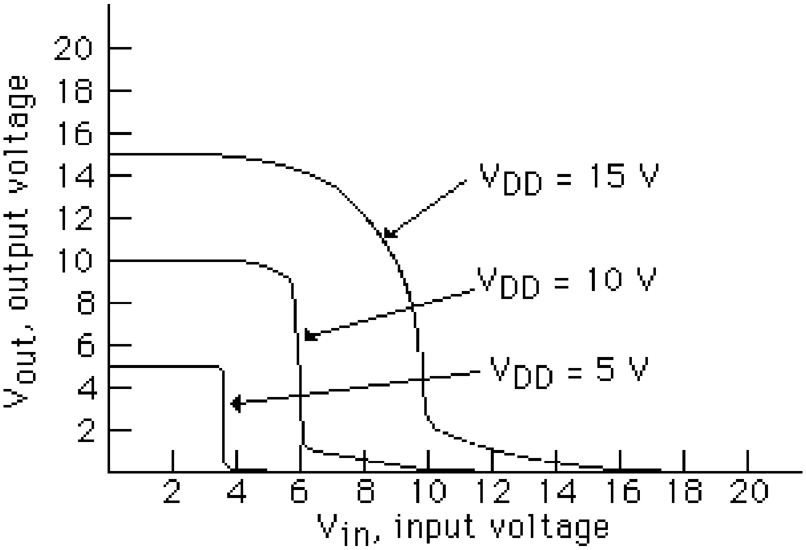


Figure 3.6 CMOS Voltage Transfer Curve.

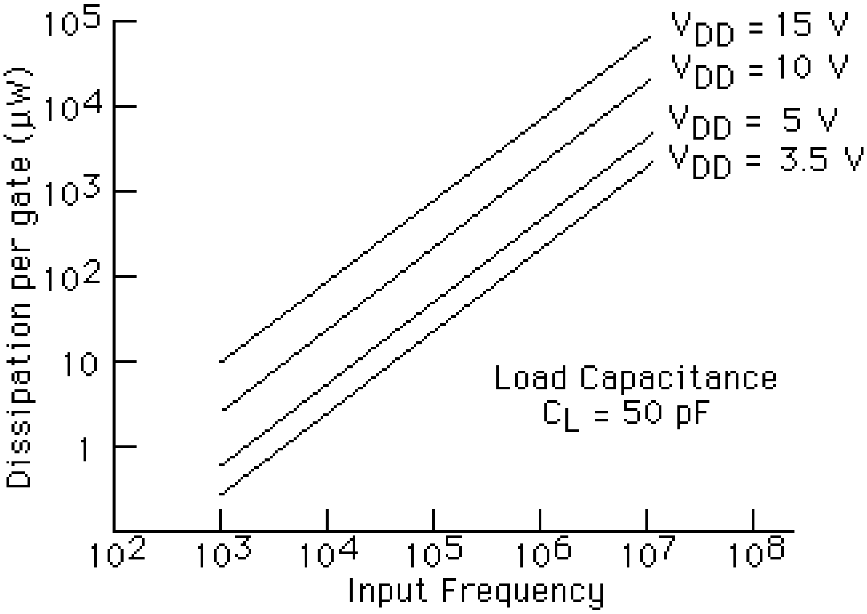


Figure 3.7 Dynamic Power Dissipation of a Typical CMOS Logic Gate.

The input **impedance**, in either state, of CMOS gates is typically 10^{12} Ω. The input capacitance is 5 pF. The output impedance depends on the particular device, and is on the order of 1 kΩ, for either state.

The **propagation delay times** for CMOS devices are relatively long due to their high output impedance. Typical delay times are 60 nsec for V_{DD} = 5 V, and 25 nsec for V_{DD} = 10 V. Doubling the supply voltage more than doubles the speed of a CMOS gate. The rise and fall transition times are typically 70 nsec. for V_{DD} = 5 V. Thus CMOS devices operate significantly slower than TTL devices.

The HIGH and LOW **noise margins** for V_{DD} = 5 V, are DC0 = V_{IL} - V_{OL} = 1.5 - 0.01 ≈ 1.5 V, and DC1 = V_{OH} - V_{IH} = 4.99 V - 3.5 V ≈ 1.5 V. In general, noise immunity is a minimum of 30% of V_{DD}, and typically 45% of V_{DD}. Thus, CMOS devices are good in noisy environments such as automobiles and industrial plants. The HIGH and LOW noise margins are essentially equal because the output impedance, output voltage, and threshold voltages are symmetrical with respect to the supply voltage.

Floating inputs in CMOS logic guarantee neither LOW nor HIGH outputs and cause increased susceptibility to noise, as well as excessive power dissipation. Hence, all unused inputs should be connected to V_{DD} or V_{SS}, as appropriate.

The **fan-out** of CMOS devices is usually greater than 50 because the input current requirement of CMOS logic is nil (~pA). However, current is required to charge and discharge the capacitance of CMOS inputs during logic transitions. Hence, the greater the fan-out the longer the propagation delay. For example, with V_{DD} = 5 V, the propagation delay will increase from 60 nsec when the output drives 1 input to 150 nsec when the output drives 10 inputs. As a rule of thumb, you can assume the load will be 5 pF per CMOS input plus 5 to 15 pF for stray wiring capacitance.

Outputs of CMOS gates, like those of totem-pole TTL gates, should never be connected together. Also, the power supply should be turned on before applying any logic signals to a CMOS device and the logic signals should be removed before turning off the power supply, otherwise the device could be damaged.

PRELAB

Wire the circuit for parts A, C and the circuits shown in part D and F. Use one CD4001 IC to implement parts A and C. One of its gates can be used for each part. Use another CD4001 IC to implement the circuit in part D. Note that the resistor used in part D can be inserted into the breadboard. The circuit in part E is a subcircuit of that in part D. The circuit in part E should be realized during lab by rewiring the circuit from part D after part D is completed. Also use the 74LS00 IC to implement the circuit in part F. The capacitor used in part F can be placed into the breadboard. The circuit in part G can be realized from part F during lab after the part F is completed.

PROCEDURE

Before performing the procedures listed below, read the report section of the experiment to assure you make all required measurements and record all required data.

Warning: Always apply power and ground before applying any input signals to CMOS devices; otherwise, the device may be damaged. Also remove any input signals to CMOS devices before removing power.

A. CMOS Operation

1. Use the logic level switches and the oscilloscope to observe the behavior of one of the CMOS gates in a CD4001 IC. Note that you **cannot** use the LED's to display the output since the LED's are designed for TTL logic. Use the oscilloscope to observe the output instead. Put your answer in your final report.

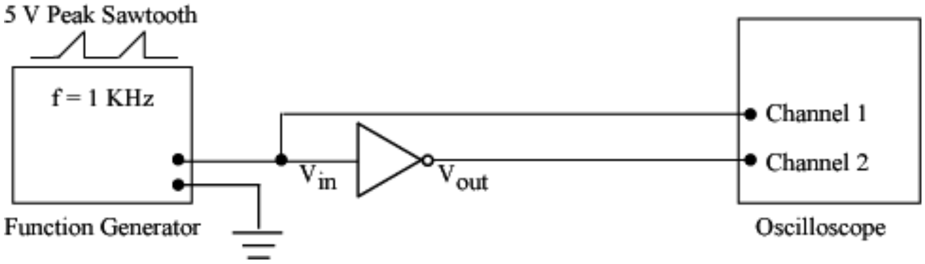
a. Observe the output of this circuit for all input combinations. From these results, give the voltage level table for the circuit; use H for HIGH and L for LOW.

b. Give the truth table for the circuit assuming positive logic. (The positive logic convention assigns a logic 1 (0) to the high (low) voltage.) What logic function is realized?

c. Give the truth table for the circuit assuming negative logic. (The negative logic convention assigns a logic 0 (1) to the high (low) voltage.) What logic function is realized?

B. Voltage Transfer Curve

1. Find the voltage transfer curve of a TTL NOT gate (74LS04) using the setup shown below:



Set the generator to produce a triangular wave of frequency 1 kHz. The duty cycle knob on the generator should be pulled out and turned completely clockwise. This will simulate a sawtooth waveform. The amplitude should be adjusted to read 2.5 V peak-to-peak on the LED display. The offset knob should be at its 12 o'clock position. Finally, the POS output mode pushbutton should be engaged to restrict the amplitude to positive voltages in the range 0 V to 5 V. ***Warning: The input waveform should never exceed 5 V peak at any time. Higher voltages***

could damage the gate. Hence, before connecting the function generator to the gate input, make certain that the amplitude of the function generator waveform does not exceed 2.5 V. Connect the gate output V_{out} to the Channel 2 input and V_{in} to the Channel 1 input of the oscilloscope. Turn on Channel 2 input by pressing the CH 2 button along the right side of the screen. In order to plot Channel 1 vs. Channel 2, press the DISPLAY menu button, then *Format YT*. This will bring up another menu along the right side of the screen. Select XY. The resulting plot of V_{out} vs. V_{in} is the gate voltage transfer curve. Be sure that the volts/div. scales are set to give a useful display. You may want to set the input couplings on Channels 1 and 2 to ground temporarily. The dot that appears on the screen indicates the zero vertical and horizontal voltage potential and should be located at the bottom left corner of the screen. Obtain a screen dump of this curve and copy it to your final report, making sure to record any important vernier settings.

2. Determine the gate threshold voltage from the voltage transfer curve.

3. Determine the DC0 and DC1 noise margins for this gate. Assume V_{OL} = 0.4 V, and V_{OH} = 2.4 V. Use the voltage transfer curve to determine V_{IL} and V_{IH}.

4. Find the voltage transfer curve of a two-input CMOS gate in the CD4001 IC using the same approach as above.

a. Insert a picture of the waveform in your final report.

b. Determine the gate threshold voltage from the curve.

C. Rise and Fall Times

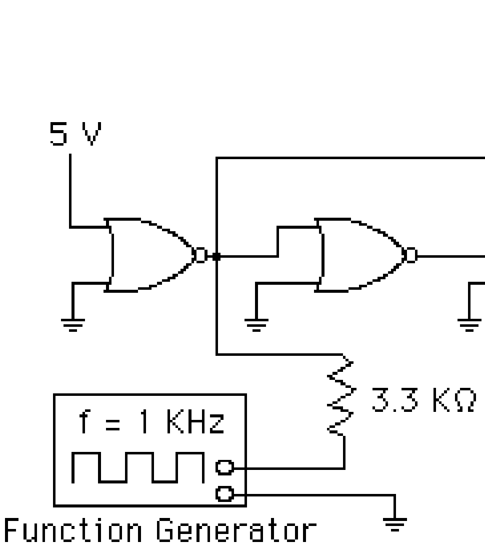
1. Apply a 307.2 kHz square wave (appendix A) from the logic box to the inputs of a CD4001 CMOS gate and to the inputs of a 74LS00 TTL gate (see Figure 3.4). Use the oscilloscope to display the outputs from both gates simultaneously. Carefully plot the output waveforms for both gates on the same axis, then copy it to your final report. Which family, TTL or CMOS, has the faster rise and fall times?

D. Noise Margin

1. Determine the DC0 noise margin for a gate in the CD4001 IC using the circuit shown in the figure below and the following procedure, and put the answer in your final report:

a. Initially, the amplitude knob on the generator should be set so that the input pulse has minimum amplitude.

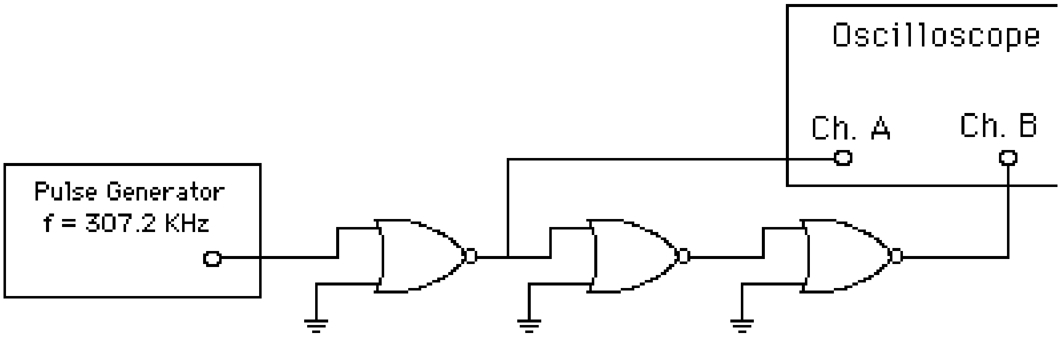
b. Carefully increase the amplitude of the input while observing its magnitude on Channel 1 (or A) of the scope. When a pulse first appears on the output, Channel 2 (or B) of the scope, then the amplitude (0 volt to positive peak value) of the input pulse is the DC0 noise margin.



Circuit to Determine Noise Margin of CMOS Gates.

E. Propagation Delay

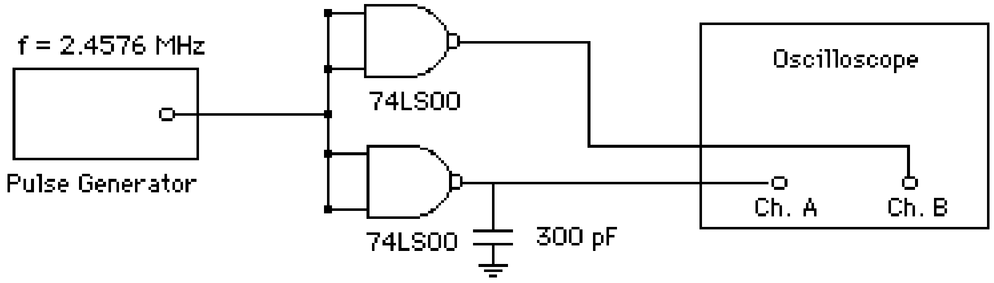
1. Find the propagation delay through two CMOS gates in the CD4001 IC using the circuit below. Use the clock pulse generator on the Logic Box. Return the oscilloscope to YT format (voltage vs. time), with both Channels 1 and 2 (or A and B) displayed on the screen. Obtain detailed close-ups of the output waveforms at the first and last gates, during both transitions from HIGH to LOW and LOW to HIGH. Copy them to your final report. Find the average propagation delay per gate.



Circuit to Determine CMOS Propagation Delay.

F. Capacitive Loading

1. Connect the pulse generator on the logic box to two NAND gates in the 74LS00 IC and a 300 pF capacitor to the output of one of the NAND gates, as shown. The capacitor will simulate the capacitive loading component induced by several gate inputs. Obtain a picture of the screen, showing the two outputs displayed simultaneously. Copy it to your final report. What is the effect of capacitive loading on rise and fall times? Determine the rise and fall times with and without capacitive loading.



G. Current Spiking

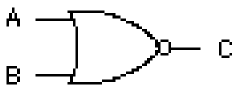
1. Disconnect the other IC's from the power supply so that only the 74LS00 IC is connected to power. Disconnect the capacitor and function generator, used in part F, from the 74LS00's NAND gate and the logic box, respectively. Set the pulse generator in the logic box to 307.2 kHz and connect it to all the inputs of all four gates on the 74LS00 IC. Observe the power supply voltage at the V_{SS} pin on the 74LS00 and the output of one of its NAND gates simultaneously on the oscilloscope. Copy the waveforms to your final report. During which transition is the spiking of the power supply greater?

EXPERIMENT 3--TTL & CMOS CHARACTERISTICS

FINAL REPORT

I. CMOS Operation

a) Complete the voltage level table from the results determined in the lab for a CMOS CD4001 integrated circuit:



A	B	C
L	L	
L	H	
H	L	
H	H	

b) What is the resulting truth table assuming positive logic? What logic function has been realized?

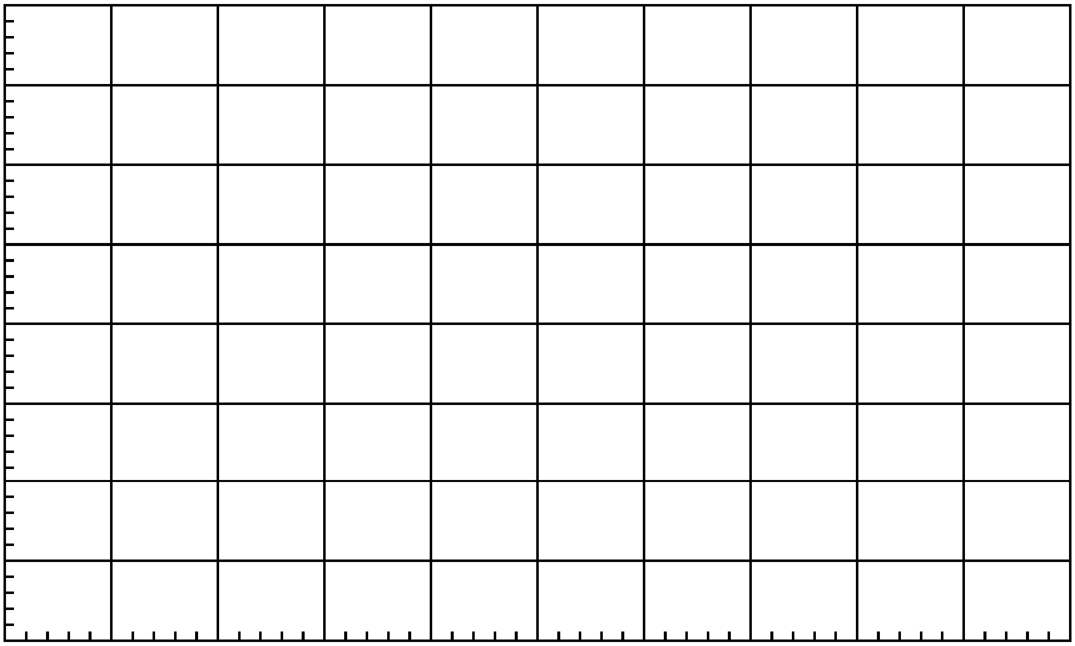
A	B	C
0	0	
0	1	
1	0	
1	1	

c) What is the resulting truth table assuming negative logic? What logic function is realized in this case?

A	B	C
0	0	
0	1	
1	0	
1	1	

II. Voltage Transfer Curve

a) Plot the voltage transfer curve of the TTL & CMOS gate as determined in lab.



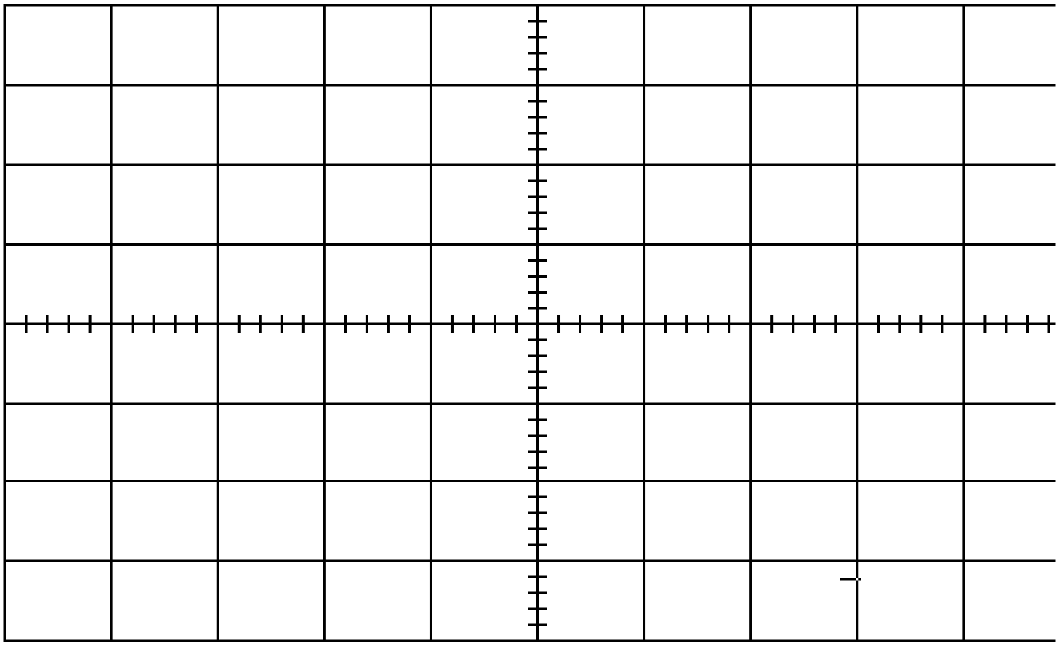
Voltage Transfer Curve of a TTL & CMOS gate.

b) On the plot above illustrate graphically the procedure for determining the gate's threshold voltage. What is the resulting threshold voltage?

c) Illustrate graphically the procedure for determining V_{IL} and V_{IH} for a TTL gate. What are the DC0 and DC1 noise margins for this gate? Show how they were determined.

III. Rise and Fall Times

a) On the graph below, plot both output waveforms resulting when a 307.2 kHz square wave is applied to a CMOS gate and a TTL gate.



Rise and Fall Times of CMOS and TTL logic.

b) Which device family for this device, TTL or CMOS, has the faster rise and fall times?

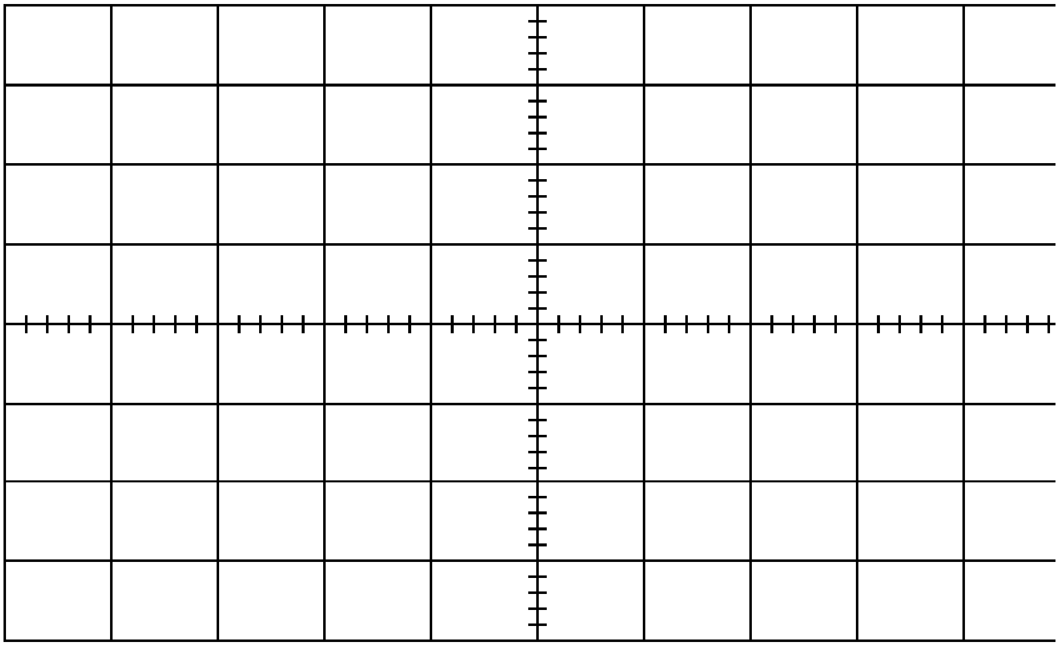
IV. Noise Margin

a) What is the DC0 noise margin measured for the CMOS gate?

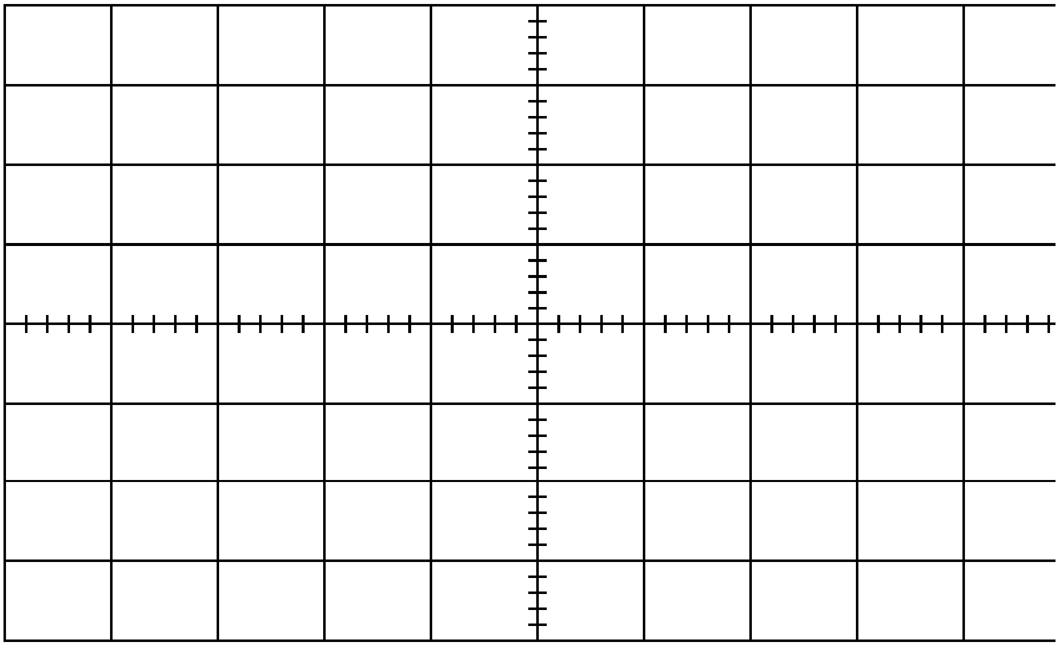
b) As a result of this measurement and the results in II c) for determining the noise margin of TTL devices, which device family would be the best candidate to use in designing digital circuits for an electrically "noisy" environment?

V. Propagation Delay

a) Plot the output waveforms observed in part E of this experiment to determine the propagation delay through CMOS gates.



Propagation Delay--LOW to HIGH Transition

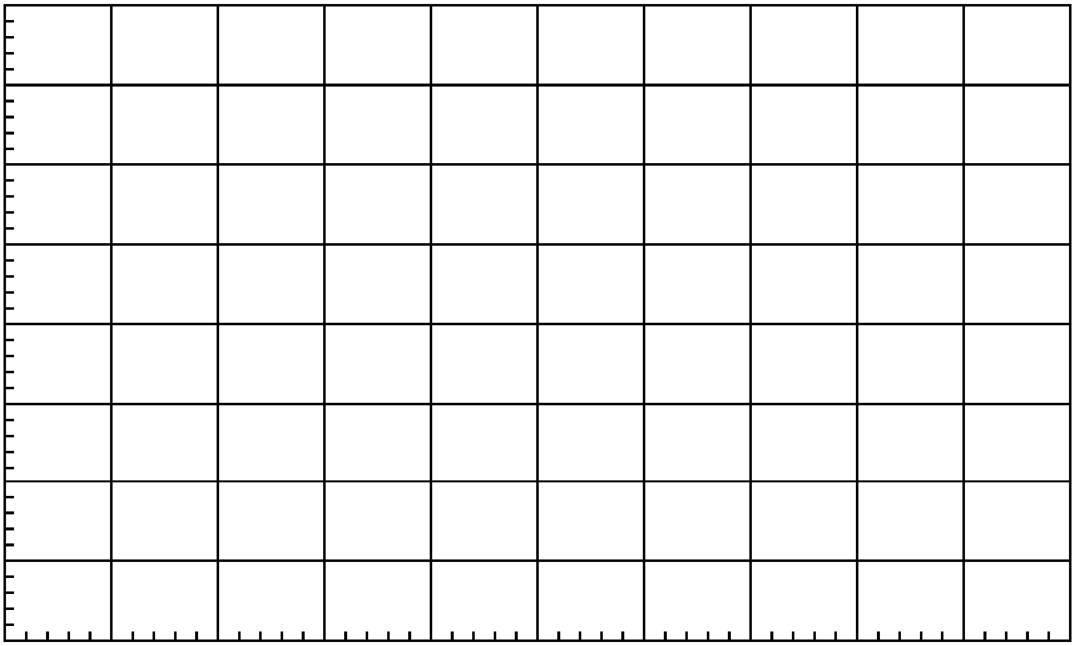


Propagation Delay--HIGH to LOW Transition

b) What is the resulting average propagation delay per gate? Indicate how it was determined. Compare it with the average propagation delay of a TTL gate (e.g., a 74LS04 inverter) as listed in a TTL data sheet.

VI. Capacitive Loading

a) Graph the two output waveforms obtained in Part F below:

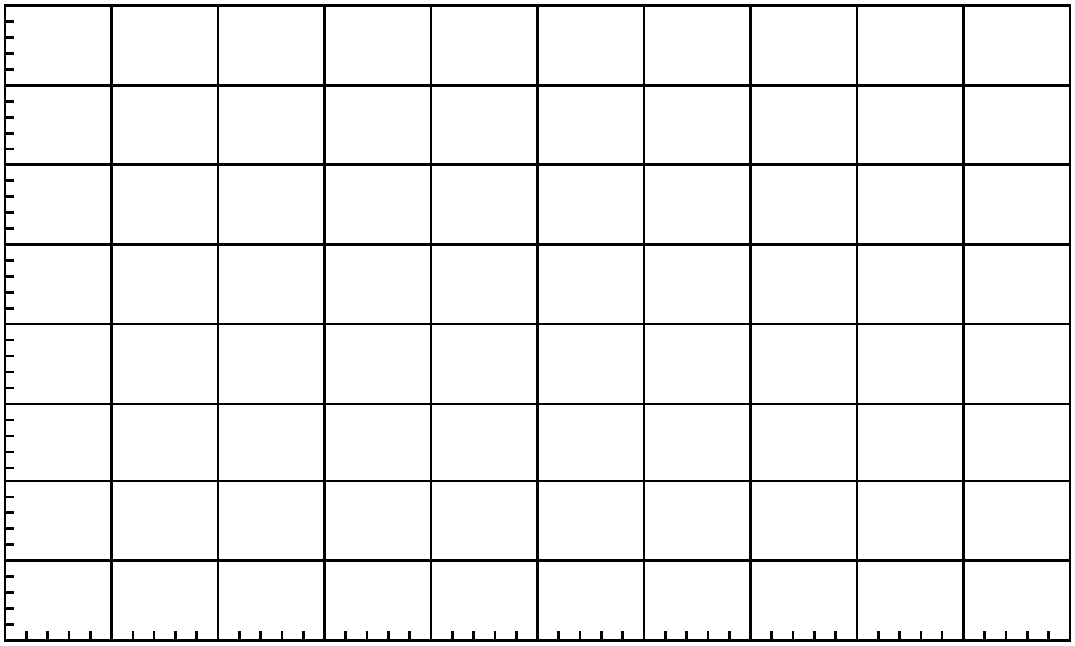


Effects of Capacitive Loading

b) What effect does capacitive loading have on the rise and fall times of gate outputs? Calculate the rise and falls times with and without capacitive loading.

VII. Current Spiking

a) Graph the gate output and voltage supply waveforms obtained in Part G.



Current Spiking

b) If this degradation of the power supply is left unchecked in large circuits, circuit operation can become impaired. The many gate outputs switching at any moment will all, for a brief moment, attempt to draw huge amounts of current simultaneously. The power supply may not be able to satisfy this sudden demand for current. How can this problem be circumvented?

VIII. Summary

Write a concise description of the device characteristics measured for TTL and CMOS logic in this experiment. Contrast the measurements for TTL with those made for CMOS. From this comparison, determine which design criteria would favor the use of TTL logic and which would favor the use of CMOS.