The CLEO II Silicon Vertex Detector

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We describe a vertex detector comprised of three layers of double-sided silicon wafers, installed in the CLEO II detector at the Cornell Electron Storage Ring (CESR). The innermost silicon wafers are located a distance of 2.35 cm from the stored electron and positron beams; the beams carry a total of 300 mA of current. Characterizations of the improvements in detector performance since VERTEX'96, results on beam related occupancy, and evaluations of detector resolutions are presented. The prospects for physics results from a data set corresponding to integrated luminosity $4\,\mathrm{fb}^{-1}$ with the device installed are discussed.

1 Introduction

The CLEO Silicon Vertex Detector (SVD), located at the Cornell Electron Storage Ring (CESR), is taking data in a rather unique and interesting environment compared to other operating silicon detectors. The CESR beam current that runs through the center of the detector is nearly 1/2 amp, which is nearly 1/2 amp greater than beam currents seen by other detectors. The inner-most layer of the CLEO SVD is only 2.35 cm from the beam while the outer-most layer is at 4.8 cm; the detector can be nearly contained inside the LEP beampipe. Data is taken at $\sim$ 35 Hz ($\sim 1\,\mathrm{pb}^{-1}\mathrm{hour}^{-1}$) and is expected to increase to 60 Hz when the CESR luminosity reaches $6 \times 10^{32}\,\mathrm{cm}^{-2}\mathrm{sec}^{-1}$ later in the year. To date, the CLEO SVD has taken $4\,\mathrm{fb}^{-1}$ of data at or near the $\Upsilon(4s)$. The initial pass over these data has begun and first results are emerging.

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2 Design of the SVD

The principal physics targets of the CLEO SVD differ somewhat from the targets of vertex detectors at other colliding beam facilities. Most prominently, when a stationary $\Upsilon(4s)$ decays to B-mesons, the B-mesons decay after traveling a mean distance of only $30\,\mu$m, which renders statistically significant event-by-event reconstruction of the B vertex nearly impractical. However, similar reconstruction of vertices from D-mesons and τ-leptons from B decay, and from continuum e^+e^- production, does form a practical target.

An application of the CLEO SVD that is distinct from uses of vertex detectors at other facilities is the reconstruction of angles of soft particle trajectories, particularly the angle θ measured from the colliding beam axis. Use of double-sided silicon positioned very close to the beam pipe allows the measurement of the z coordinate of a particle trajectory in the direction parallel to the beam axis, prior to degradation of that coordinate caused by multiple coulomb scattering in the beam pipe and successive silicon layers. When combined with a constrained fit to a primary or event vertex, the CLEO SVD allows reconstruction of θ from soft particles, such as the slow π from $D^{\star+}$ decay, that is limited by tracking resolution, and not multiple scattering.

The momentum spectrum of particles produced at $\sqrt{s} \approx 10\,\text{GeV}$ is soft, and peaks at only a few tenths of a GeV, so the resolution in the extrapolation of particle trajectories back to the e^+e^- annihilation point, or impact parameters, is usually dominated by the contribution from multiple coulomb scattering in the beampipe and inner layers of silicon. The minimization of the beampipe radius, therefore, minimizes the impact parameter resolution. Although the stored beam current is typically 300 mA, careful radiation shielding design has allowed the CLEO beampipe to be reduced to a 2 cm radius, permitting the placement of the first layer of silicon at a radius of 2.35 cm. A total of three layers was chosen, to provide high efficiency for measurement of at least two hits: the second layer is at a radius of 3.25 cm, and the third is at of 4.75 cm.

The layout of the SVD is shown in Figure 1, in projections perpendicular to the beam axis (the $r\phi$ projection) and parallel to the beam axis (the rz projection).

Each silicon wafer has implants on both sides, with n-implants facing the beam axis, and arranged perpendicular to the beam axis, to measure the z coordinate of a particle trajectory. On the opposite side, away from the beam axis, p-implants parallel to the beam measure the ϕ coordinate. The detector is comprised of 96 silicon wafers, and contains 26,208 channels.

3 Silicon Detectors and Front-end Electronics

The dimensions of our double-sided silicon wafers are summarized in Table 1.

Table 1
CLEO SVD wafer specifics.

	Layer 1	Layer 2	Layer 3
Radius (mm)	23.5	32.5	46.9, 48.1
Active Half Length (mm)	59.5	76.4	119.1
Active Width / Side (mm)	21.2	28.9	21.2
Active Thickness (μm)	300	300	300
Number of J/CAMEXes / Side	3	4	3
Readout Strips / Side	189	252	189
Number of Hybrids / Octant	1	1	2
$r\phi$-side (p implant)			
Implant Pitch (μm)	28.0	28.5	28.0
Readout Pitch (μm)	112	114	112
Strip Capacitance (pF)	9	11	18
Amplifier Chips	CAMEX	CAMEX	CAMEX
z-side (n implant)			
Implant Pitch (μm)	105	101	105
Strip Capacitance (pF)	28	34	56
Number of Sense Strips	567	756	1134
Amplifier Chips	CAMEX	CAMEX	JAMEX

The p-implants have a pitch of about 28 μm, and every fourth implant is read out. The n-implants have a pitch of near 100 μm and every one is instrumented.

Both sides of the wafer are AC-coupled, with the capacitor formed by a layer of insulator and a trace of metallization above the implant. On the side with n-implantation, an additional upper layer of metallization is placed above the capacitive readout layer, in order to lead the signals out to the front end electronics located at the end of the detector. Each upper metallization trace is connected to three readout strips. This additional upper layer of metallization adds capacitance to the n-side readout, and is responsible for a reduced signal to noise for that side.

All wafers were manufactured by Hamamatsu Photonics [2]. There are five fundamental layouts, to accommodate mirror-image situations. For the wafers in the outermost layer, pairs of silicon wafers are glued end-to-end, and bridging wirebonds are made to produce a double-length detector. The front ends are CAMEX64 VLSI chips [3], except on the rz side of the outermost layer, where the JAMEX64 [4] is used. The input noise is $350 + 30 \cdot \mathrm{C_d}(\mathrm{pF})$ in ENC for the CAMEX64, where $\mathrm{C_d}$ is the detector capacitance, and the coefficient of $\mathrm{C_d}$ is about 15 ENC/pF for the JAMEX64.

4 Mechanical Features

The 96 silicon wafers are assembled into 8 mechanical units, each containing 12 wafers, known as octants, evident in Figure 1. Each octant is suspended from one of a pair of hemi-cylindrical supports fabricated of carbon fiber composite, known as clamshells. Most of the structural integrity comes from the staircase-shaped supports in each octant that are fabricated from beryllium oxide, shown in the lower portion of Figure 1; these supports are outside the fiducial tracking volume, and attached with precision pins to the clamshell.

The thick-film hybrids, built also on beryllium oxide substrates, which carry the front-end electronics for the silicon detectors, are permanently epoxied between successive segments of the stair-case shaped beryllium supports. The silicon detectors themselves are permanently epoxied to the hybrids.

In the fiducial region, the silicon wafers are supported by U-channels made of Kevlar composite. The U-channels are glued to the wafer faces with intermittent epoxy beads, to allow easy shear between the silicon and the support. Shear arises from thermal strain from the small mismatch between the silicon and fiber coefficients of thermal expansion.

The fiber supports contribute a thickness of about 0.22% of a radiation length in the fiducial volume, to be compared with 1.2% of a radiation length for the silicon wafers themselves.

The front-end electronics generate $\sim 200mW$ of heat per chip, and beryllium oxide was chosen for the hybrid substrates and staircase support because of its excellent heat conduction; the staircase supports additionally provide some ballast to slow thermal incidents. Epoxy loaded with boron carbide was used to assemble the supports, in order to provide good heat conduction. A freon cooling loop in contact with the extremities of the beryllium oxide supports, as well as water cooling in the beampipe itself, ultimately remove the heat generated by the electronics.

Assembly of the wafers, hybrids, and supports was performed with a series of fixtures mounted on pairs of precision-aligned platens. Alignment of pieces to about 25 μm was held during assembly, although ultimately it was foreseen to rely on alignment with tracks from the data itself.

5 Signal to Noise

Signal to noise (S/N) is a basic parameter for any silicon detector; it impacts the efficiency, the occupancy and the resolution. The CLEO SVD was designed to have a signal to noise ratio from 14 to 20 for the $r\phi$-sides and 10 to 13 for the z-sides. Table 2 shows the results of two measurements of the CLEO SVD signal to noise. The first measurement was made just after commissioning of

Table 2
Signal to noise measurements before and after colliding beam data was taken.

	Layer 1	Layer 2	Layer 3
Cosmic Ray Data			
$r\phi$ (p implant)	18	14	11
z (n implant)	10	8	10
Colliding Beam Data			
$r\phi$ (p implant)	13	11	10
z (n implant)	10	9	10

the detector using cosmic ray data and the second measurement was made with colliding beam data. The signal to noise performance was reduced in

Table 3
Signal spreading as measured with data.

	Layer 1	Layer 2	Layer 3
$r\phi$-side (p implant)			
Nearest neighbor	$9.7\% \pm 0.3\%$	$9.0\% \pm 0.3\%$	$8.1\% \pm 0.4\%$
Next nearest	$1.33\% \pm 0.04\%$	$1.54\% \pm 0.05\%$	$2.1\% \pm 0.1\%$
Total	$22.0\% \pm 0.6\%$	$21.0\% \pm 0.6\%$	$20.4\% \pm 0.8\%$
z-side (n implant)			
Nearest neighbor	$2.5\% \pm 0.3\%$	$1.7\% \pm 0.4\%$	$0.8\% \pm 0.4\%$
Total	$5.0\% \pm 0.6\%$	$3.4\% \pm 0.8\%$	$1.6\% \pm 0.8\%$

colliding beam conditions. These degradations are a result of modifications made to the timing and triggering scheme and poor control signal shaping and have caused an artificial increase in the pedestal widths for all channels. An upgrade to rectify the problem is currently underway and is expected to be finished by the end of September 1997. The pedestal widths are expected to be reduced significantly.

The signal to noise ratio is also influenced by the ability to efficiently reconstruct the charge deposited by tracks. Signal spreading can influence charge and has been found to be a sizeable effect in the CLEO SVD. The signal spreading on the $r\phi$-side was measured with normally incident tracks that passed midway between readout strips. Ideally, equal amounts of charge would be seen on the nearest strips and none in the outside neighbors. However, the charge on the outside neighbors was found to be linearly correlated with the charge on the hit strips. The effect is quite large on the $r\phi$-side, where roughly 20% of the charge deposited on a strip is spread to its neighbors. The z-side signal spreading was measured in a similar fashion, except that the normally incident track had to pass under a readout strip to insure single strip pick-up. The z-side sharing is less dramatic and has been determined that only $\sim 3\%$ of the deposited charge is spread to the neighbors. Table 3 shows the amount of signal spreading as a function of layer and side for the CLEO SVD.

Table 4
A breakdown of the exceptional channel occupancy in the CLEO SVD.

	Disconnected	Broken Hybrids	Too Noisy to Start a Cluster	Total
Layer $1r\phi$	1.0%	0.0%	2.1%	3.1%
Layer $2r\phi$	2.0%	0.0%	2.3%	4.3%
Layer $3r\phi$	3.3%	0.0%	3.7%	7.0%
Layer $1z$	0.6%	0.0%	4.7%	5.3%
Layer $2z$	1.5%	6.3%	3.9%	11.7%
Layer $3z$	2.6%	6.3%	3.9%	12.8%

6 Efficiency

The efficiency of a silicon detector is dictated primarily by the channels that are defective, on broken detectors or have large pedestal widths. Data in channels with large pedestal widths are sometimes removed from the data stream by the online zero-suppression algorithm, resulting in inefficiencies. The zero-suppression algorithm used at CLEO is based on a predetermined list of the exceptional channels. Noisy channels are flagged in calibration as exceptional if their pedestal widths are greater than 6000 electrons or if their widths differ from the chip average by more than a factor of 2. Pedestal widths for normal channels range from 1600 to 2500 electrons, depending on layer and side. Channels with large pedestal widths are not allowed to start or finish a cluster, but are otherwise treated as a normal channel by the zero-suppression algorithm. Table 4 gives the frequency of occurrence for the three types of exceptional channels.

An interesting comparison can be made between the exceptional channel rates and the hardware inefficiencies. Figure 2 is a plot of the hardware inefficiencies as a function of side, layer and end of the SVD. The plot is summarized in Table 5.

The inefficiencies on the $r\phi$-sides fall below the exceptional channel rates, due, most likely, to the high S/N, absence of clumping of the exceptional channels, and cross talk between adjacent channels; the converses are all true for the z-side, where the inefficiencies track the exceptional channel rates. The hardware efficiencies by layer/side can be seen in Table 6. The efficiencies reported at the VERTEX‘96 Workshop [1] are included for comparison. The increase in efficiency since last year’s workshop is a direct result of better

Table 5
Comparison of the measured hardware inefficiencies and exceptional channel rate.

	Measured Inefficiency	Exceptional Channels
Layer $1r\phi$	$0.5\% \pm 0.1\%$	3.1%
Layer $2r\phi$	$1.8\% \pm 0.1\%$	4.3%
Layer $3r\phi$	$4.9\% \pm 0.2\%$	7.0%
Layer $1z$	$4.5\% \pm 0.2\%$	5.3%
Layer $2z$	$11.0\% \pm 0.3\%$	11.7%
Layer $3z$	$13.5\% \pm 0.4\%$	12.8%

Table 6
Comparison of the measured efficiencies reported at the VERTEX‘96 Workshop and the most current ones. The current efficiencies give an expected two-hit-per-view fraction of 98%.

	Vertex‘96	Vertex‘97
Layer $1r\phi$	0.957 ± 0.008	0.995 ± 0.001
Layer $2r\phi$	0.947 ± 0.008	0.982 ± 0.001
Layer $3r\phi$	0.854 ± 0.014	0.951 ± 0.002
Layer $1z$	0.799 ± 0.014	0.955 ± 0.002
Layer $2z$	0.791 ± 0.014	0.890 ± 0.003
Layer $3z$	0.759 ± 0.015	0.865 ± 0.004

global calibration procedures.

7 Occupancy

Occupancy is the fraction of strips that are read out per event. The occupancy of the CLEO SVD is approximately 5% and is derived primarily from four sources – incoherent noise ($\sim 2\%$), extra edge strips kept in clustering ($\sim 2\%$), beam related occupancy ($\sim 2\%$) and physics ($< 0.1\%$). Calibration drift results in a time dependence in the incoherent occupancy and is monitored in real time to insure that valid constants are always being used.

The large incoherent contribution to the occupancy is due to the relatively

Table 7
This table shows the size of the variations we have observed in calibrating the CLEO SVD.

	Layer 1	Layer 2	Layer 3
Channel to Channel Gain Variations			
$r\phi$ (p-implant)	$2.65\% \pm 0.05\%$	$2.78\% \pm 0.04\%$	$5.29\% \pm 0.07\%$
z (n-implant)	$3.43\% \pm 0.06\%$	$4.63\% \pm 0.07\%$	$12.92\% \pm 0.28\%$
Chip Gain Variations			
$r\phi$ (p-implant)	$1.8\% \pm 0.2\%$	$1.9\% \pm 0.2\%$	$3.5\% \pm 0.3\%$
z (n-implant)	$2.3\% \pm .3\%$	$3.8\% \pm 0.4\%$	$5.2\% \pm 0.6\%$

low thresholds used in the zero-suppression algorithm. The thresholds are low in order to keep the efficiency high, especially on the z-side. Under current conditions, most of our channels have pedestal widths between 1600 and 2500 electrons. Cluster edge thresholds are set at 2000 electrons and a cluster must have at least 8000 electrons of charge in order to enter the CLEO data stream. If a cluster passes these criteria, extra strips at the edge of the clusters are kept if they have at least 1000 electrons.

Table 7 is a breakdown of the calibration variations that have been measured. The electronic pulser calibration system was used to determine the channel to channel gain variations in the detector and were found to be small except in the case of the JAMEX64. The minimum ionization peak in Bhabha events determines the overall gain for each of the J/CAMEX chips. Comparing the chip gain values over several months revealed that there is no global offset in these constants but there is some drift to them.

8 Resolution

The intrinsic resolution of the device is evaluated using μ-pair events. A single track constraint is imposed in the fit of the pair in order to reduce the track extrapolation error in the residuals. The remaining track extrapolation error in the residuals has been approximated from simulation and accounted for in the reported resolutions. Figure 3 is a plot of the intrinsic resolution as function of entrance angle.

The $r\phi$-side intrinsic resolution gets better as the the track inclination increases due to the increase in the effective signal to noise since the signal grows as $1/\sin\theta_{\rm track}$. The z-side intrinsic resolution function has three interesting features. There is a minimum in resolution as a function of $\theta_{\rm track}$ and occurs at the fiducial limit for single strip acceptance ($\tan^{-1}(100\mu{\rm m}/300\mu{\rm m})$). The resolution at normal incidence is 29 μm ($100\mu{\rm m}/\sqrt{12}$) and is strictly determined by strip pitch. The amount of signal charge per unit length of traversed wafer in z falls as $1/\cos\theta_{\rm track}$ thus reducing the effective signal to noise.

9 Results

The CLEO SVD has been used to observe and measure the dynamic beta effect at CESR. The oppositely charged particles in the CESR beams are attracted to each other via the coulomb interaction and this attraction causes the beam profile to be squeezed as the beams pass through each other. The amount of distortion to the beam profile is dependent on the amount of current in each beam. This is the dynamic beta effect and is most easily measured in the horizontal plane. The results can be seen in Figure 4 and is the first observation and measurement of this effect.

The CLEO SVD was designed to resolve D meson and τ lepton vertices at CESR. Currently, we have $\sim 4\times10^6$ τ-pair events and $\sim 21\times10^6$ D decays with silicon information. The first pass over the silicon era data has recently started and first results are emerging. Figure 5 is a plot of the $D^\pm$ mass peak before and after a flight length cut is used to maximize signal significance, where the flight length is calculated using the $D^\pm$ vertex and the run-by-run beam centroid. The signal significance is improved by a factor of 10 with a flight path cut at 7 times the resolution in flight path.

10 Summary

The CLEO SVD has successfully acquired 4 fb^{-1} in the challenging conditions at CESR and is expected to see another ~ 5 fb^{-1} in the months to come. The device is in close proximity to 300 mA beams and has been used to make the first measurement of the dynamic beta effect. The hardware efficiency continues to improve while currently yielding a 98% two-hit-per-view tracking efficiency. The signal to noise ratio is high enough to do physics but current upgrades will improve the situation significantly. The intrinsic resolutions have been evaluated and are well understood. The signal significance of a sample of $D^\pm$ decays has been improved by one order of magnitude by use of silicon.

References

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[3] G. Lutz, W. Buttler, H. Bergmann, P. Holl, B.J. Hosticka, P.F. Manfredi and G. Zimmer, NIM A263 (1988) 163.

[4] G. Lutz, F. Maloberti, P.F. Manfredi, V. Re, V. Speziali, W. Buttler, H. Vogt, NIM A264 (391-398) 1988.

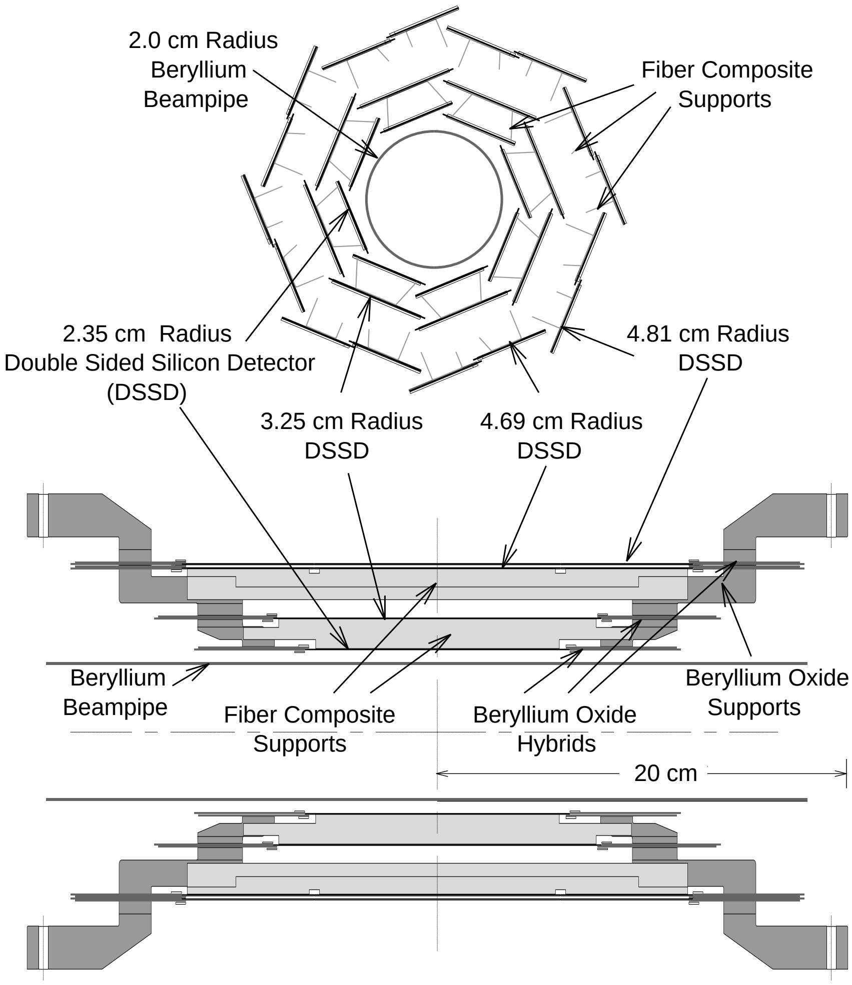

Fig. 1. CLEO SVD cross-sectional $r\phi$ view (top) and rz view (bottom).

The $r\phi$ layout is octagonal, with overlap in the corners, to provide efficiency and the ability to align the detector. In the rz projection, a pairs of wafers meet with no overlap at the detector center, and are read out at either end. About 92% of the solid angle is covered by the detector.

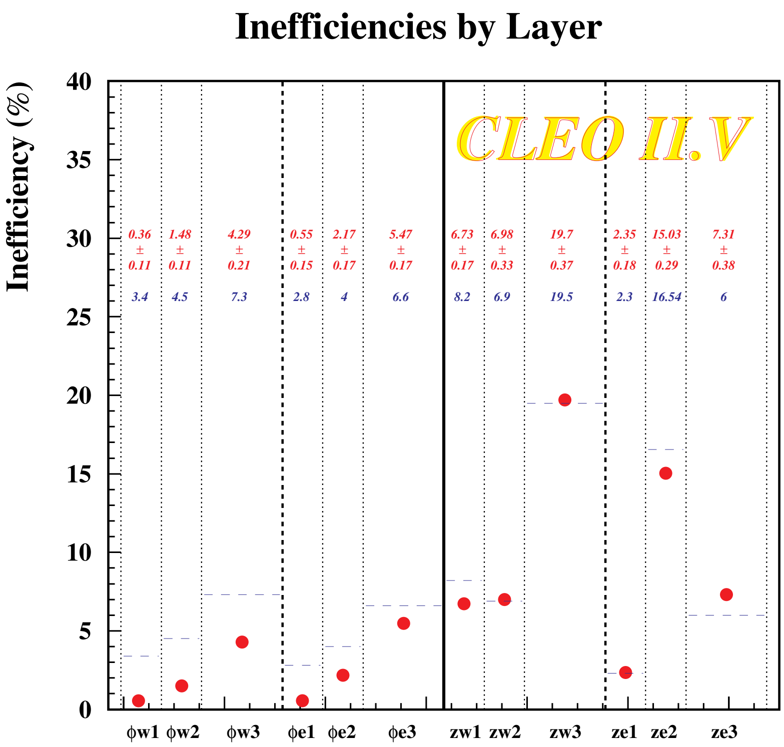

Fig. 2. Hardware inefficiencies in the CLEO SVD. The first six points are the inefficiencies for the $r\phi$ side, layers 1,2 and 3 in the east end of the detector and then layers 1, 2 and 3 in the west end. The next six points are the inefficiencies for the z side. The lines represent the exceptional channel rates at each of the data points.

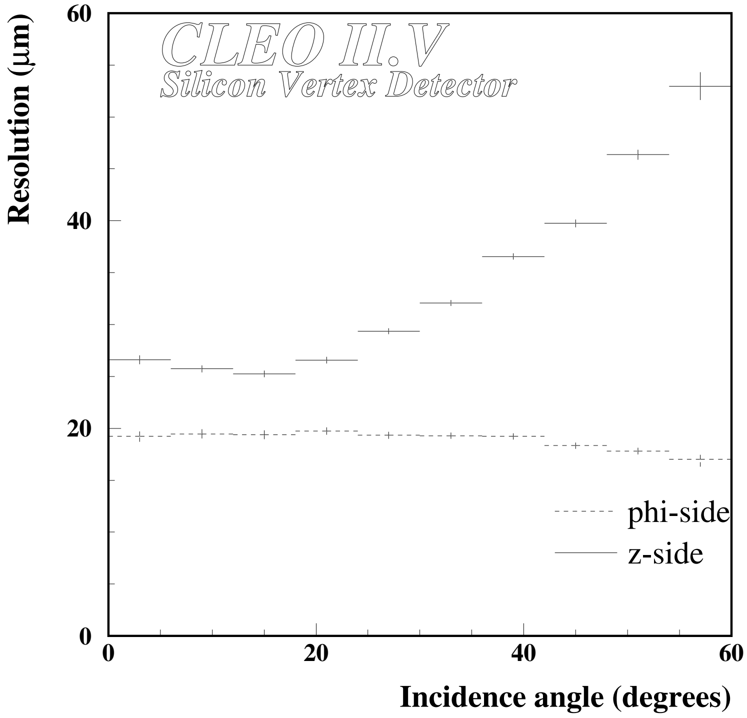

Fig. 3. Intrinsic device resolution as a function of track incidence angle.

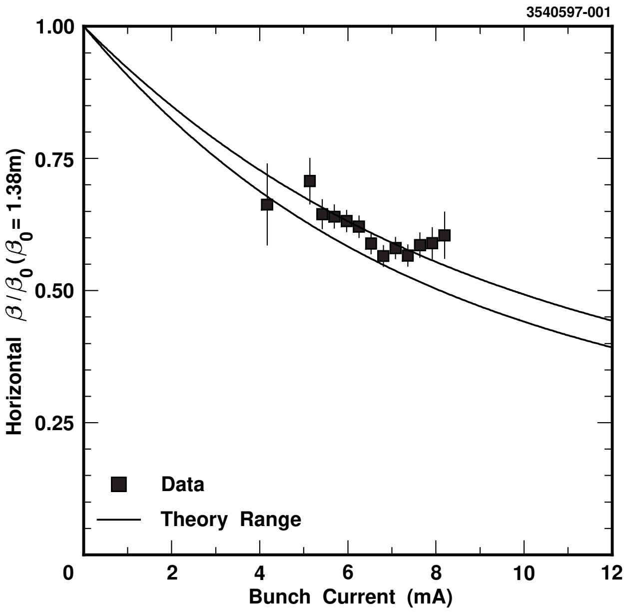

Fig. 4. First measurement of the dynamic beta effect. CLEO SVD was used to measure the effect at the CESR storage ring.

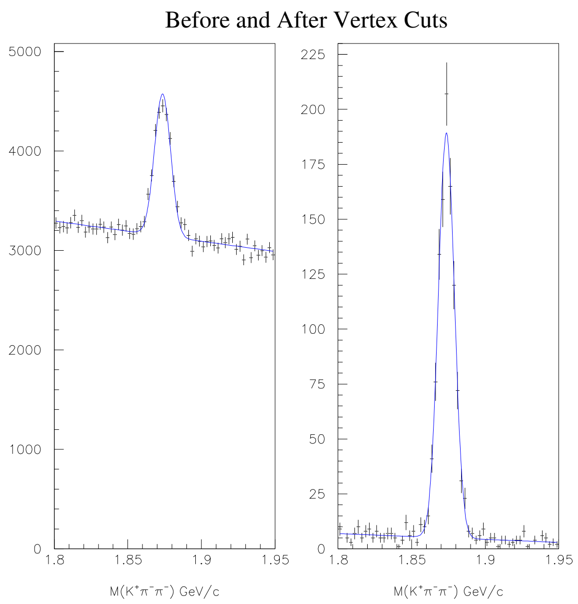

Fig. 5. $D^{\pm}$ mass peak before any cuts (left) and after applying a flight path cut of 7σ (right) calculated with the run-by-run beam centroid.