Cornell digital LLRF system

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- System description
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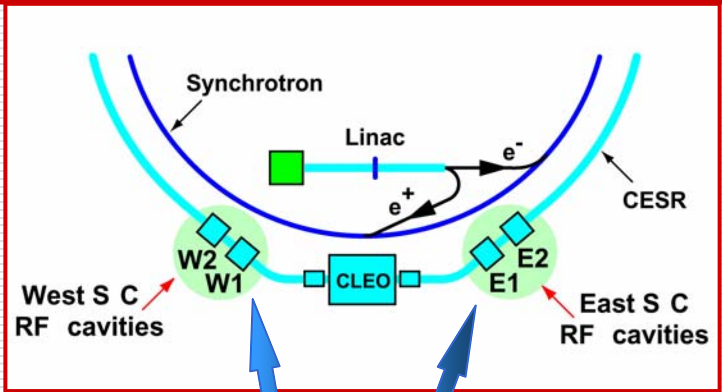
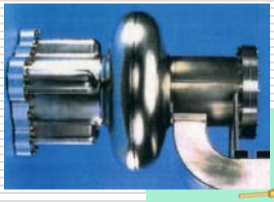
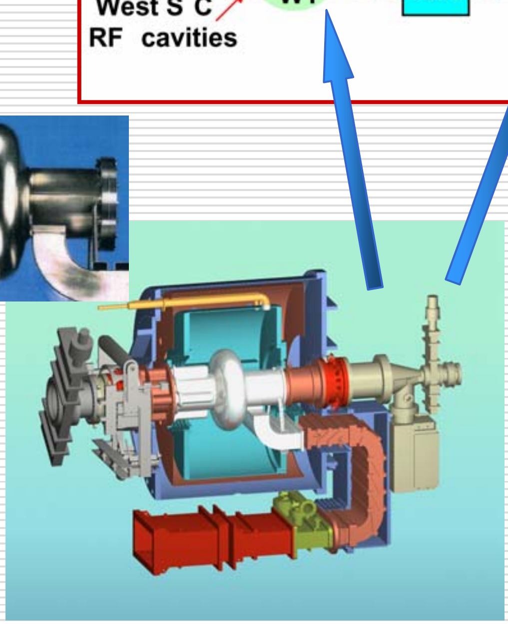
- Summary

CESR RF system



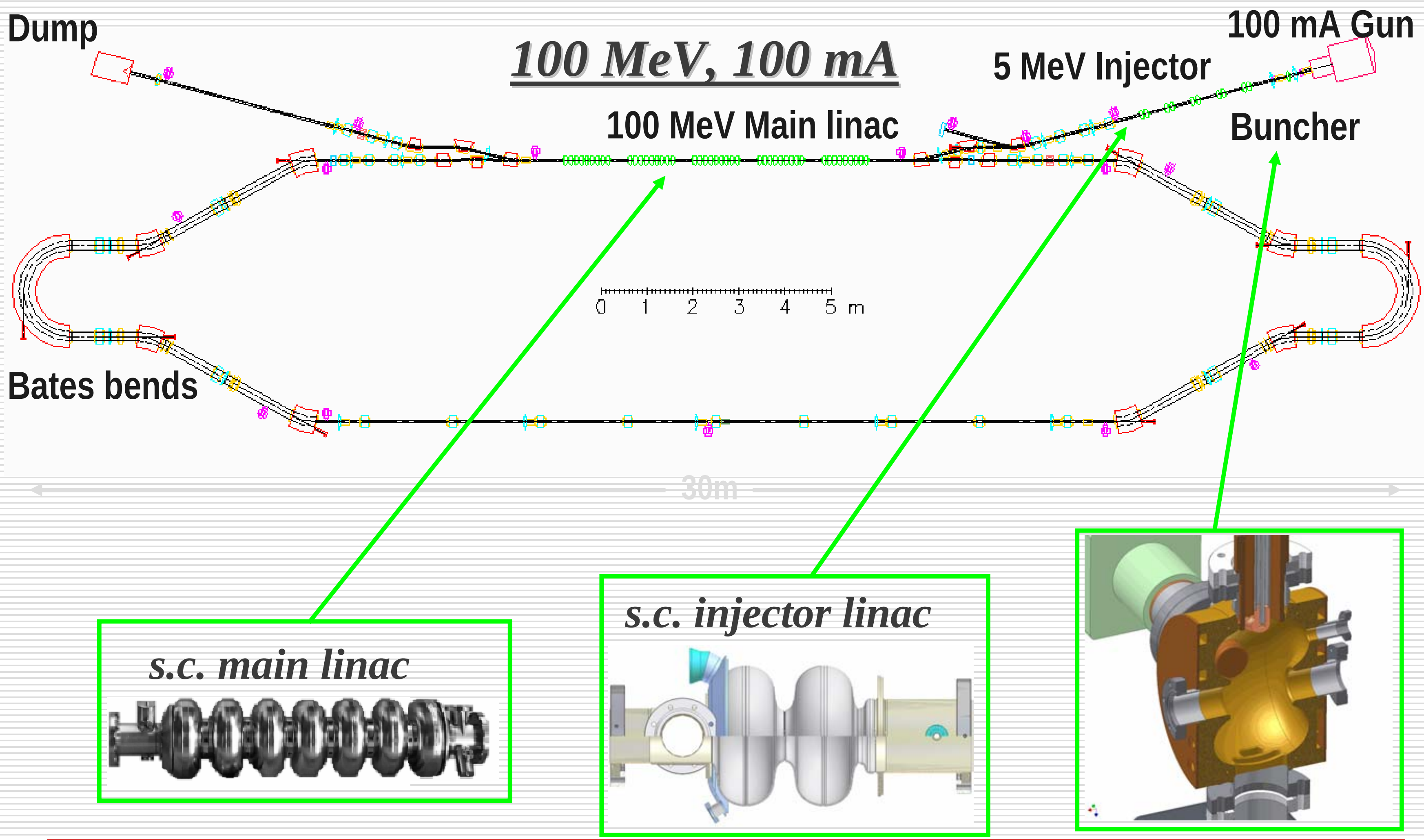
- CESR is a e^+e^- storage ring operating in two regimes: as a collider and as a synchrotron light source
- Four superconducting single-cell RF cavities
- Two cavities are driven by one klystron in parallel
- High beam loading → low loaded *Q* factor





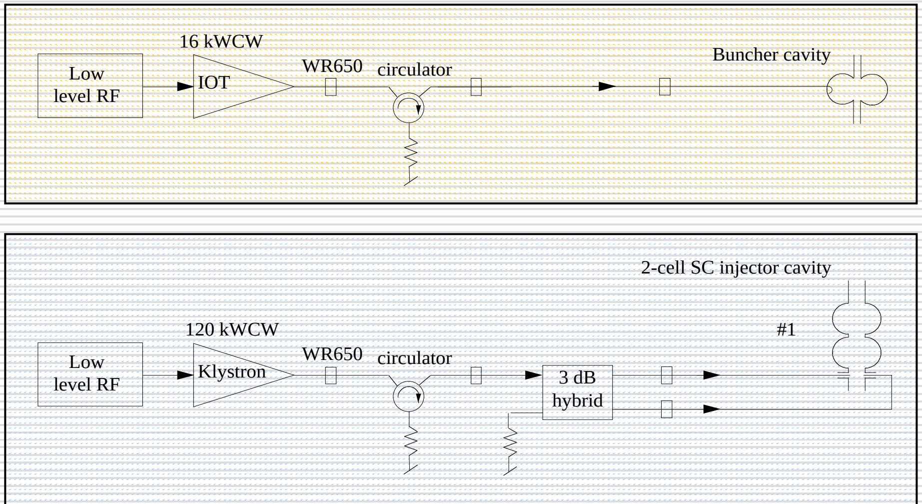
Beam energy	1.5 to 5.6 GeV
Beam current	0 to 500 mA
Frequency	500 MHz
Number of cavities	4
R/Q per single-cell cavity	89 Ohm
Q_{loaded}	2×10^5 to 4×10^5
Accelerating voltage per cavity	1.4 to 3 MV
Klystron power per cavity	up to 200 kW
Number of klystrons	2
Required ampl. stability	< 1%
Required phase stability	< 0.5°

Cornell ERL prototype



Cornell ERL RF systems

ERL Injector RF system



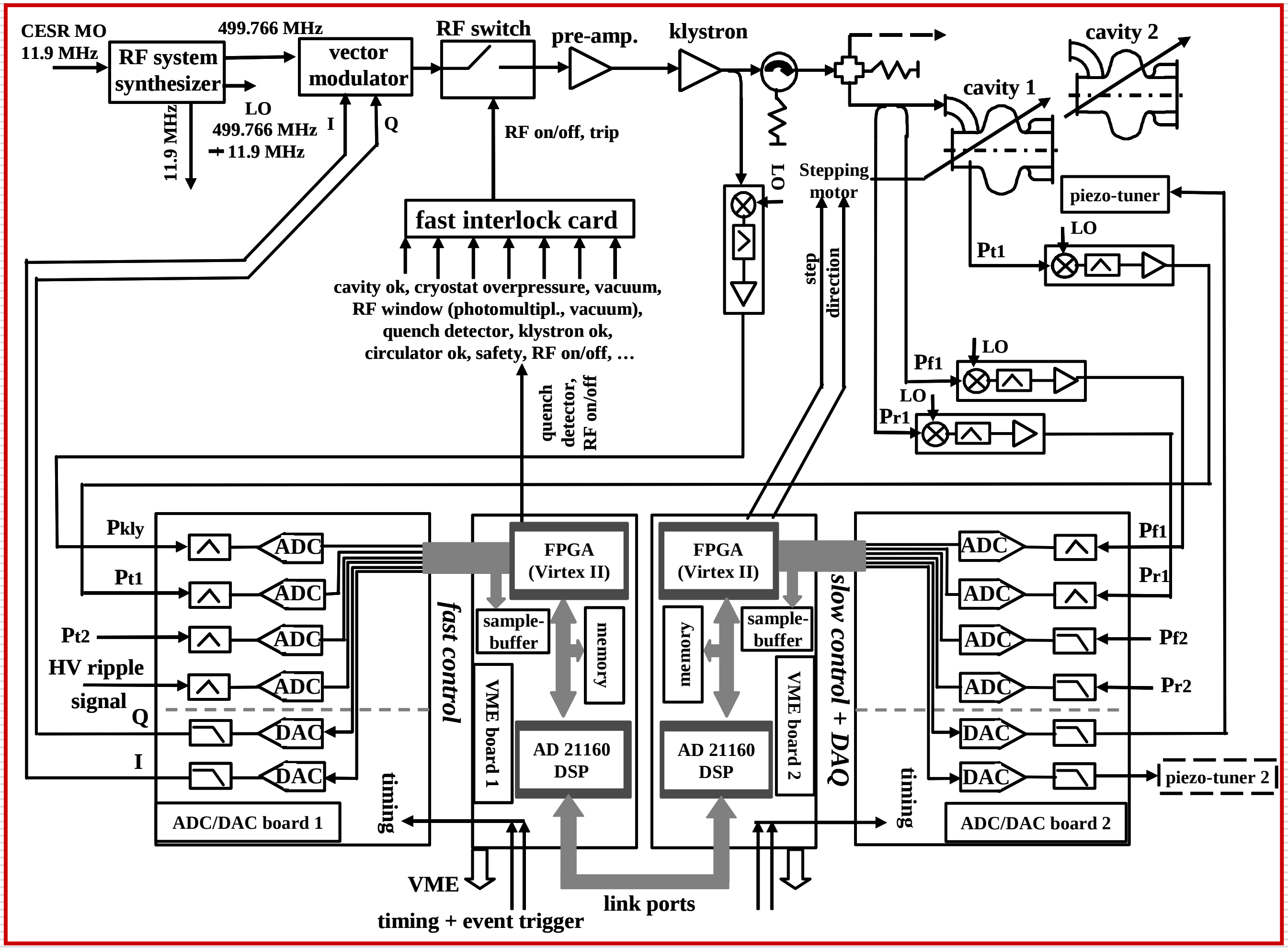
- Three distinct RF systems
- Buncher RF (single-cell normal conducting cavity): 16 kW CW IOT xmtr, prototype for the linac RF (7-cell SC cavities
- Injector cryomodule RF: 120 kW CW klystron, 2-cell SC cavities

	Buncher cavity	SC injector cavities	SC linac cavities
Frequency [MHz]	1300	1300	1300
Accelerating voltage [MV]	0.12	1 to 3	≈ 20
Q_{loaded}	2×10^4	4.6×10^4 to 4.1×10^5	2.6×10^7 (for 25 Hz peak microphonics)
Klystron power per cavity [kW]	7.9	132	≈ 14
Ampl. Stability (rms)	8×10^{-3} (bunch length)	9.5×10^{-4} (energy fluct.)	3×10^{-4} (timing jitter)
Phase stability (rms)	0.1° (energy fluct.)	0.1° (energy fluct.)	0.06° (timing jitter)

Motivations

- Replace aging analog controls of the CESR RF system with a more modern, easily upgradeable system
- Make the new system more flexible as CESR switched from a fixed-energy operation to a multiple-energy regime, which required frequent adjustment of RF control system parameters
- The new system is also a "prototype" system for ERL $\rightarrow$ design should be generic enough to be easily adaptable to other applications
- Improve diagnostics
- Add new features (piezo-tuner controls, HV PS ripple compensation,…)

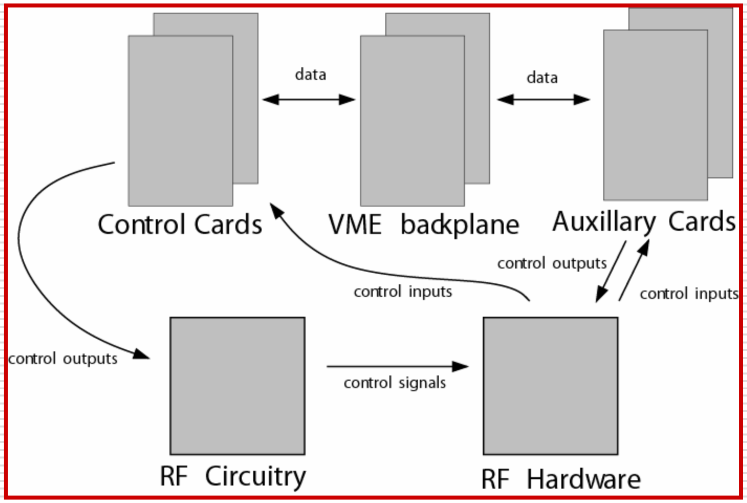
System description: Block diagram



The system includes:

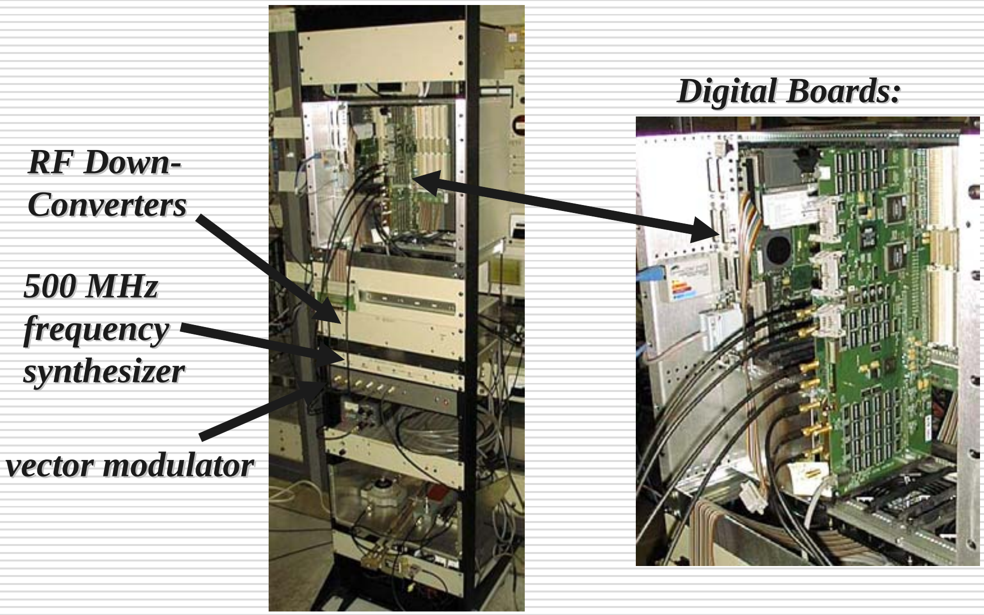
- State machine
- Vector sum control of two heavily beam-loaded cavities in CESR
- Trip and quench detection
- Adjustable klystron HV
- Tuner control (stepping motor and piezo)
- Feed-forward compensation of the HV PS ripple
- Pulsed operation for processing
- Passive cavity operation
- Diagnostics
- Link ports (high speed parallel ports) serve for data exchange between digital boards

System description: Hardware



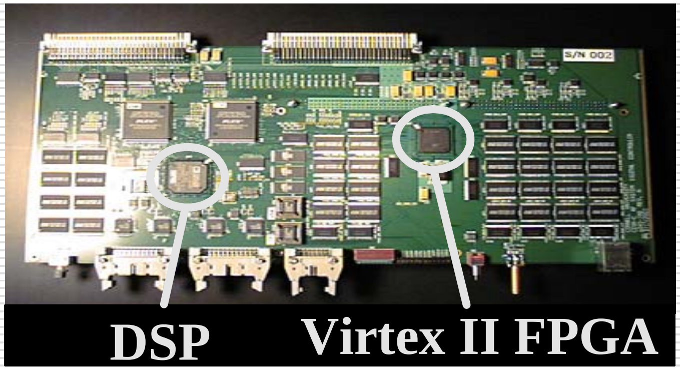
<u>The system hardware can be divided into five parts</u>:

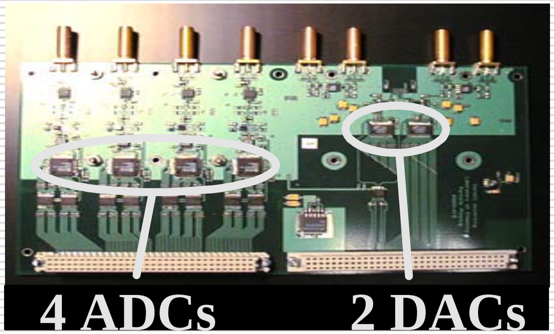
- Two controller cards (each includes a processor board and an ADC/DAC daughter board)
- VME backplane and CPU
- Auxillary VME cards (a Xycom XVME-542 ADC card and a serial XBUS interface card)
- RF circuitry (vector modulator)
- RF Hardware (drive amplifier, klystron, transmission lines, tuners, mixers,…)



System description: Controller card

- Very low delay in the control loops
- FPGA combines speed of an analog system and the flexibility of a digital system
- High computational power allows advanced control algorithms
- Both boards have been designed in house
- The controller is designed to stabilize I and Q components of the cavity field. The RF signals are converted to IF of 11.9 MHz and then sampled at a rate of 4×11.9 MHz.
- Generic design: digital boards can be used for a variety of control and data processing applications





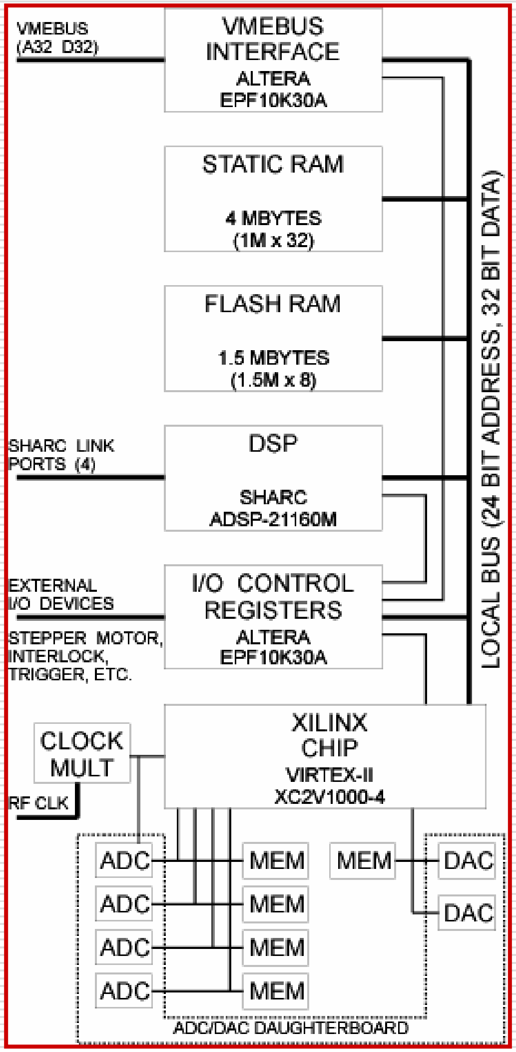
System description: Controller card boards

Processor board:

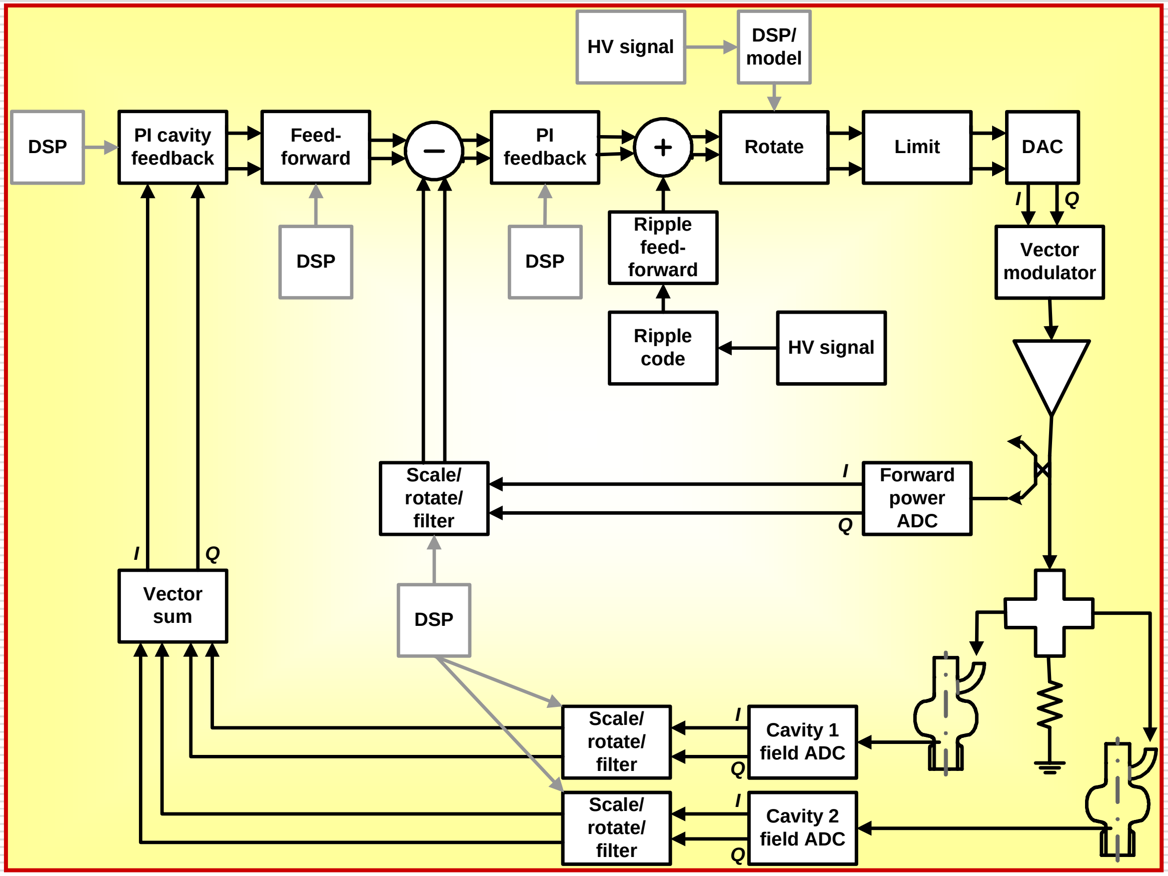
- 4 MB of fast static RAM and 1.5 MB of flash memory.
- The DSP is an Analog Devices SHARC ADSP-21160N. The chip serves as the CPU and I/O processor for the board: it performs all tasks that can be run at 100 kHz or slower.
- The FPGA chip is a XILINX VIRTEX-IIXC2V 1000-4. The fast control loops and data acquisition control run in this chip.
- Each ADC (AD6644) channel is provided with 2 MB of buffer memory. Incoming data from the ADC are stored in this ring buffer (1 Megasample each).
- A separate memory buffer is provided for the dual functions of storing data directed to the DACs (LT1668) and for a Look-Up Table for feed-forward constants.

ADC/DAC daughter board:

- Four 14-bit 65 MHz ADCs and two 50 MHz DACs
- High (74 dB) signal-to-noise ratio



System description: FPGA Software



FPGA#1:

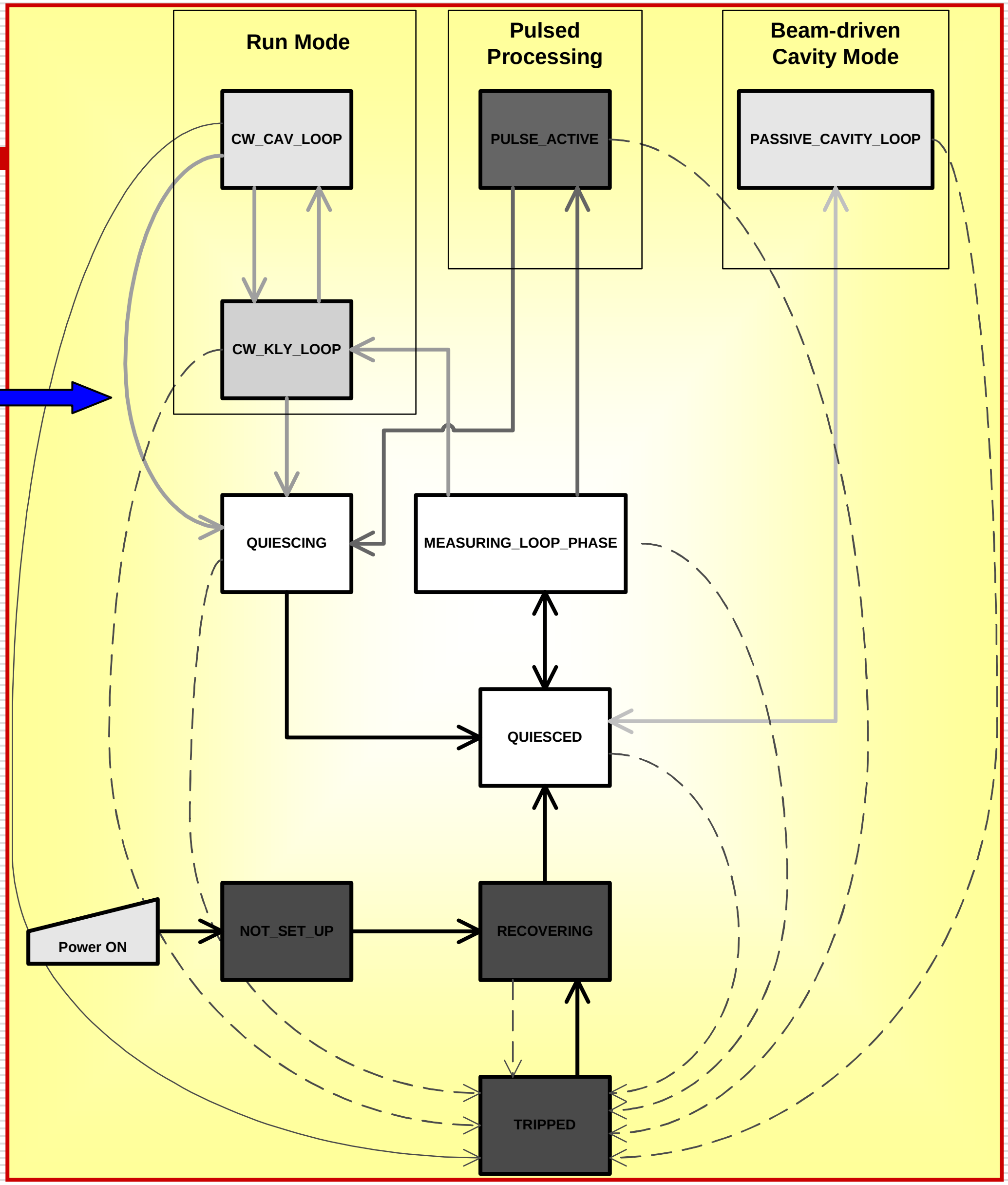
- DAQ of klystron power, cavity field signals and HV signal (DC coupled)
- True vector sum control of the fields of two cavities: proportional-integral (PI) gain cavity loop with reduced bandwidth to avoid feedback at the synchrotron frequency
- PI control loop for the klystron output (~50 kHz bandwidth)
- Fast klystron high voltage ripple feed-forward

FPGA#2:

- Only DAQ (filter and rotate/scale) of forward and reflected power signals for both cavities

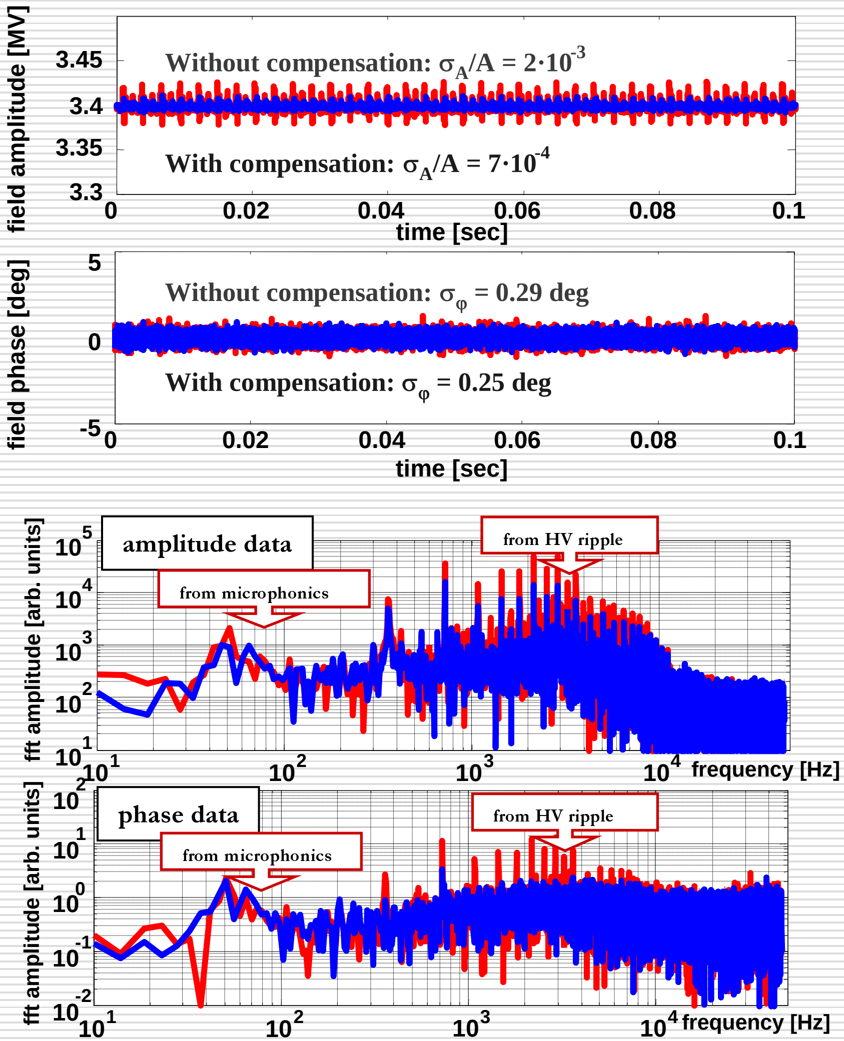
DSP software

- **DSP#1** runs the state machine, part of the fast loop and part of the slow loop.
- **DSP#2** performs data acquisition functions and runs part of the fast and slow loops.
- The **state machine** is responsible for auto-startup, auto-calibration and trip recovery.
- **Data acquisition**: DSP#2 filters and decimates 100 kHz data down to 1 Hz, performs 1 Hz peak detection on 10 kHz decimated channels.
- The **fast loop** (100 kHz): Trip and quench detection, interlock (DSP#1); Pulse generation for cavity/input coupler processing (DSP#1); synthesizer (during pulsed processing, DSP#1) and piezo DAC handling (DSP#2).
- The **slow loop** (10 kHz): Tuning angle calculation, stepping motor tuner handling, advanced piezo controls (DSP#2); Vacuum feedback for pulsed processing to adjust pulse height and length (DSP#1); Klystron handling (calculation of the power demand for HV change and rotation matrix to compensate the klystron phase shift, DSP#1)

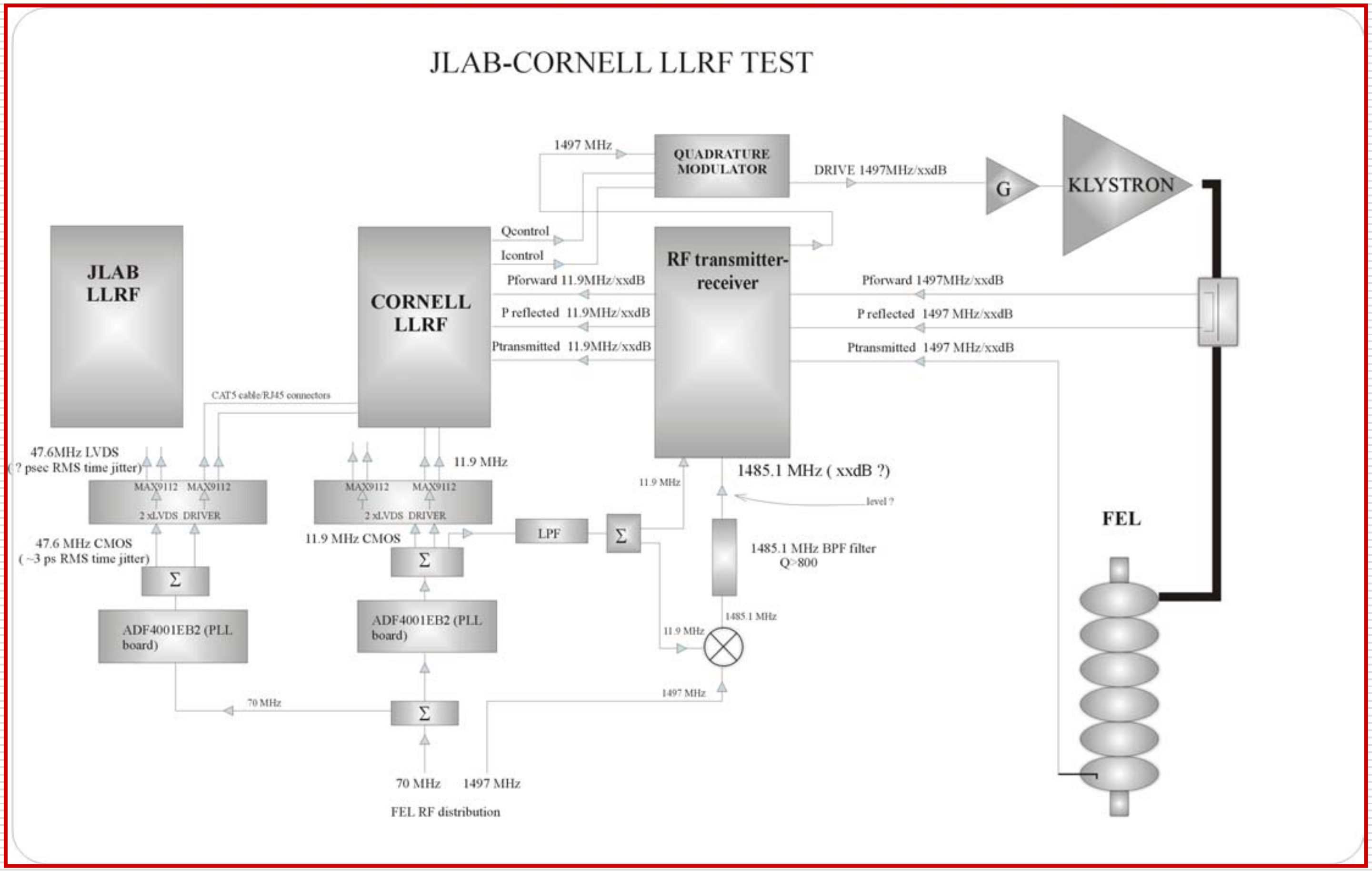


Opeartional experience in CESR

- Digital LLRF system has been in operation at CESR since summer 2004. It is very reliable.
- Achieved field stability surpasses requirements.
- System allows easy switch from operation with a loaded *Q* of 2×10^5 at high beam energy to a higher loaded Q (4×10^5)operation at low beam energy.
- Klystron high-voltage ripple is the dominating field perturbation. Feedforward compensation proved very effective.
- Phase fluctuation is dominated by the CESR reference signal noise



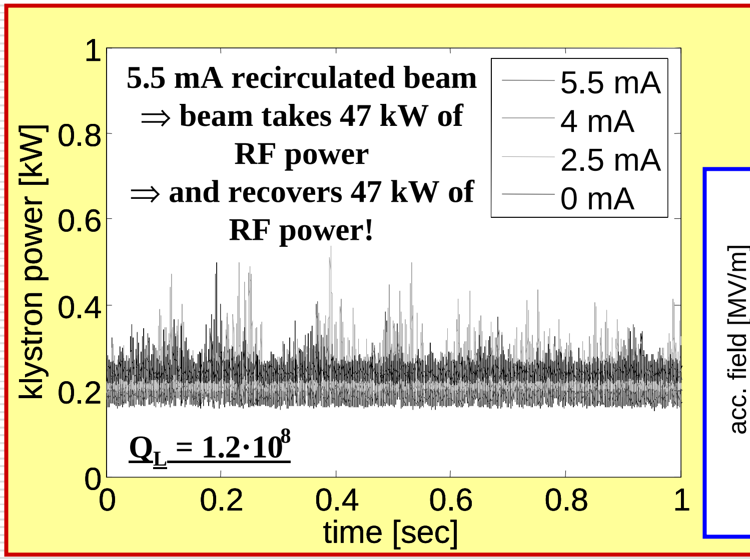
Experiments at JLab

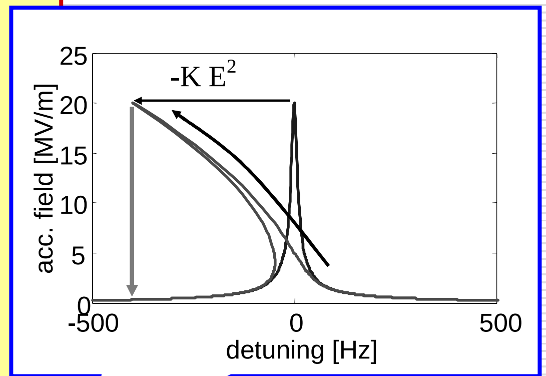


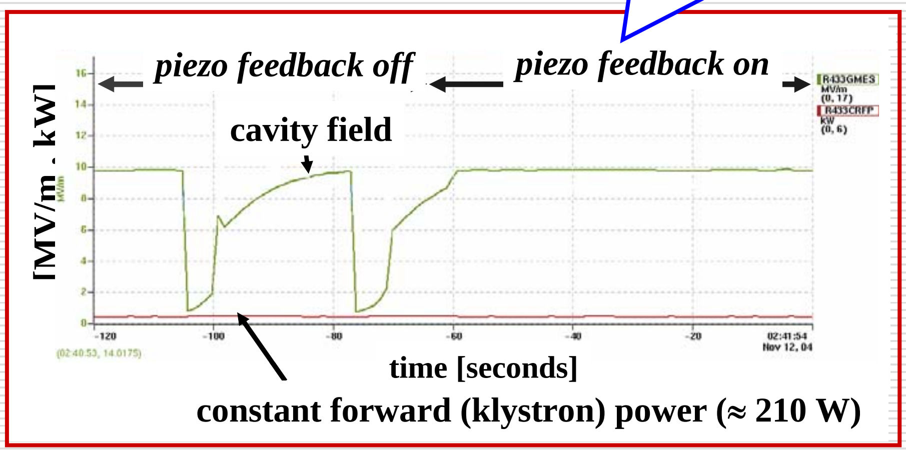
We want to operate ERL at the highest possible loaded *Q* for the most efficient operation of the RF system. We have brought our system to Jefferson Laboratory to perform a proof-of-principle experiments in collaboration with our colleagues. The JLab engineers built all the necessary RF hardware to connect the Cornell digital LLRF system to one of the 7-cell SC cavities in the FEL/ERL accelerator and to one of the 5-cell SC cavities in CEBAF.

FEL/ERL test results: High Q (1.2×10^8) operation

- Operated the cavity at Q_L= 2×10^7 (75 Hz bandwidth) and 1.2×10^8 (12 Hz bandwidth) with 5 mA energy recovered beam.
- Had the following control loops active: PI loop for the cavity field (I and Q components); stepping motor feedback for frequency control; piezo tuner feedback for fast frequency control.
- Achieved cavity field amplitude stability of 8×10^{-5} (at Q_L= 2×10^7) and 1×10^{-4} (at Q_L= 1.2×10^8) at 12.3 MV/m.
- Achieved cavity phase stability of 0.02°.
- With active piezo tuner were able to ramp the cavity field to 12 MV/m in less than 0.1 second at Q_L= 2×10^7 and in less than 1 second at Q_L= 1.2×10^8.
- Only with piezo feedback on could stabilize the cavity field at >10 MV/m.



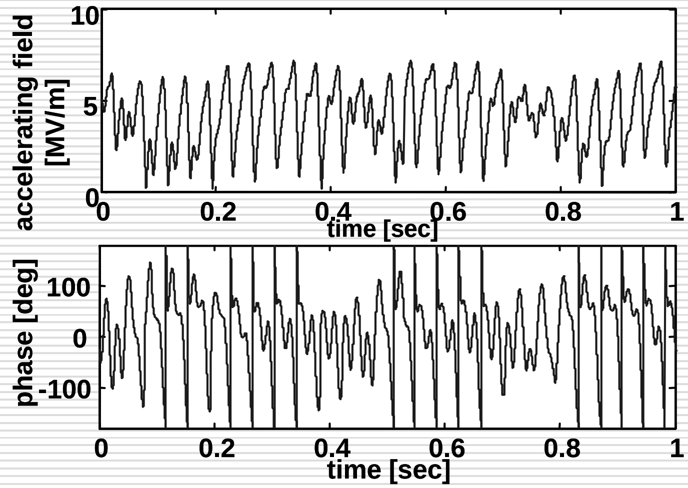




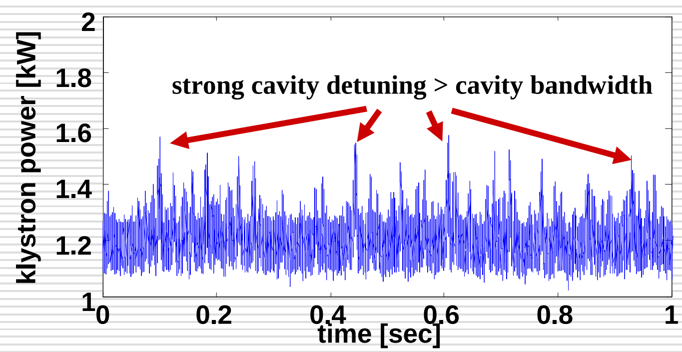
CEBAF test results: Fighting microphonics

- Increased the cavity loaded Q to 4.2×10^7 (36 Hz bandwidth) from nominal value of about 2×10^6 and ran the machine with beam current up to 4×100 µA = 400 µA.
- The chosen cavity is one of the most microphonically active cavities in CEBAF with the peak detuning more than 1.5 times the cavity bandwidth.
- We were able to close the feedback loop and achieved cavity field amplitude stability of 1×10^{-4} and phase stability of 0.01° at 10 MV/m.

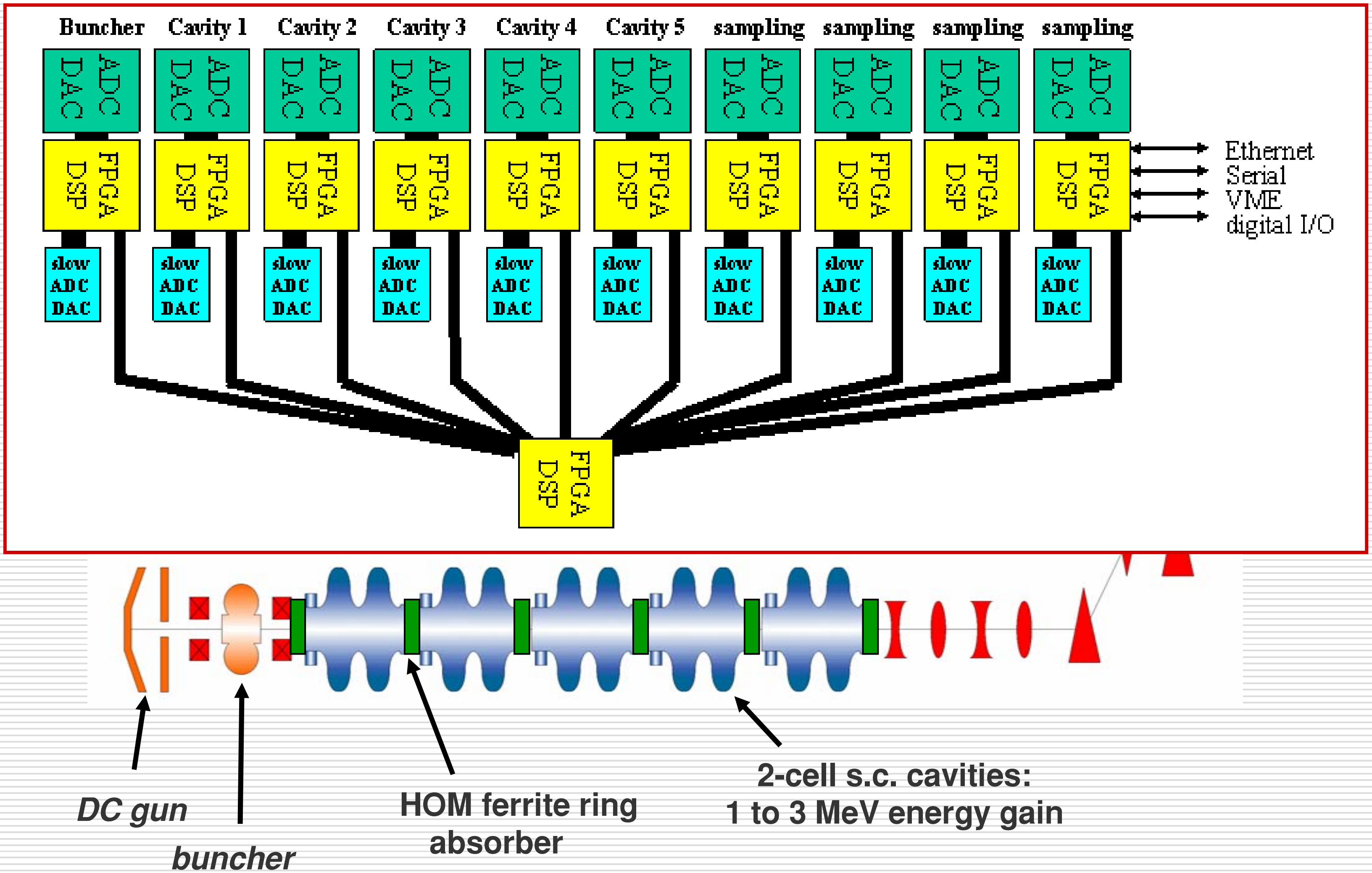
Open loop



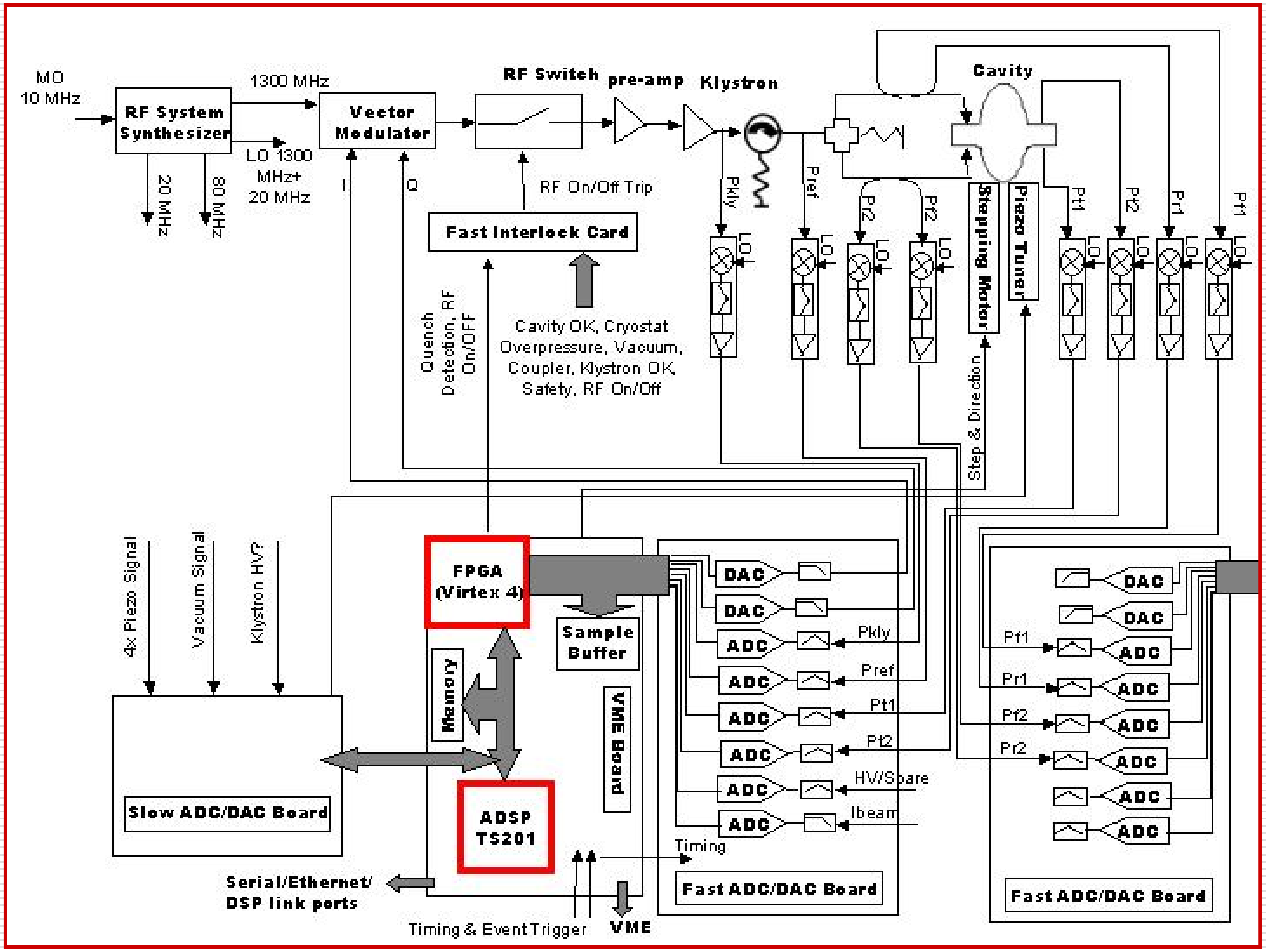
Closed loop



LLRF for Cornell ERL: System configuration



LLRF for Cornell ERL: Block diagram



Summary

- We have designed and built a digital LLRF control system
- The system is based on an in-house developed digital and RF hardware
- It features very fast feedback and feed-forward controls, a state machine and extensive diagnostics
- The first system has been in 0peration at CESR since summer 2004, surpassing requirements
- It was tested at JLab with a high loaded Q cavity and in an energy-recovery regime
- The system is generic enough to be suitable for a wide variety of accelerator applications
- The second generation is under development for use in the Cornell ERL

Acknowledgements

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